INDUCTORS IN LTCC UTILIZING FULL TAPE THICKNESS FEATURES

by

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ABSTRACT

Inductors have been produced in LTCC in a unique manner that increases the cross-sectional area of the conductor. The method uses metal-filled trenches and cavities in the tape to create conductors which are as thick as an entire layer of tape. This geometry helps to compensate for high-frequency non-idealities such as skin effect, current crowding, and proximity effect. An array of test structures has been fabricated. The measured results achieved inductors with Qs of 60 and suggest that Qs up to 100 are possible. Accurate measurements of such values require careful consideration of error sources and are discussed. A potential application of the inductors is presented in a two-pole filter, which has been modeled and fabricated. Lastly, a list of conclusions which would be helpful for future work on this subject is presented.

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"Piled Higher and Deeper" by Jorge Cham

SECTION I - INTRODUCTION

1.1 OBJECTIVE

The objective of this research is to study the feasibility of implementing high quality-factor (Q) inductors in Full Tape Thickness Feature (FTTF) Low Temperature Co-fired Ceramic (LTCC) by designing an array of inductor structures and variations and evaluating their potential for future applications. Portions of this work have been taken from a paper previously published by the author [1].

1.2 WHY THIS RESEARCH IS NEEDED

1.2.1 THE PROBLEM

High-Q inductors are necessary in order to create the clean, sharp, and narrow filters needed for a RF communication system to achieve its best possible performance. This issue is of particular concern for the design of RFIC systems. Anyone who has ever worked with inductors integrated into their IC design understands that there are serious limitations to their applications. Integrated inductors have tight restrictions on their size and traditionally have had very low Qs due to thin metal traces and substrate-induced losses.

To combat these problems, surface-mount discrete inductors may be used, or spiral inductors may be printed on to LTCC or other board substrates. LTCC is often preferred for high performance applications which allow for the chip to be directly mounted to the substrate and connected via short bondwires. Because of the layered nature of LTCC, these inductors can be located on any level of the substrate to free up surface space. While the added parasitics can still be a problem, board level inductors have the advantage over on-chip spirals of relatively unlimited size. In addition, the traces are somewhat thicker in LTCC than what is available in an IC process. For the process used in this work, traces are ~.3mil thick while all of the metal layers in an IC process combined may only be .1-.2 mil thick. More importantly, LTCC components are free of the I^2R losses caused by currents in the semiconductor substrate that degrade the performance of on-chip components so strongly. Nevertheless, their performance is still limited by the geometry of a spiral inductor and dimensions of the traces, which are still very thin in comparison to their widths.

1.2.2 MULTI-LAYER SPIRALS

Improvements can be made over the classic single-layer spiral LTCC inductor by moving from a planar structure to a 3-dimensional one such as shown in Figure 1.1. In [2] a solenoid was approximated by making turns of the inductor in LTCC printed metal with vias connecting one turn to the next. This method has shown improvements over classic planar spiral inductors in LTCC [3] but is still limited by the same problem plaguing other options; the

nature of the thin, wide traces makes it susceptible to current crowding and resulting high series resistance and degraded Q [4].

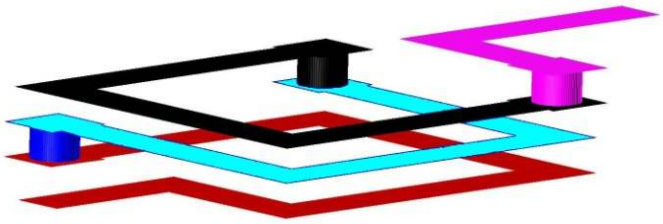


FIGURE 1.1: A TYPICAL HELICAL INDUCTOR MADE FROM THIN METAL TRACES.

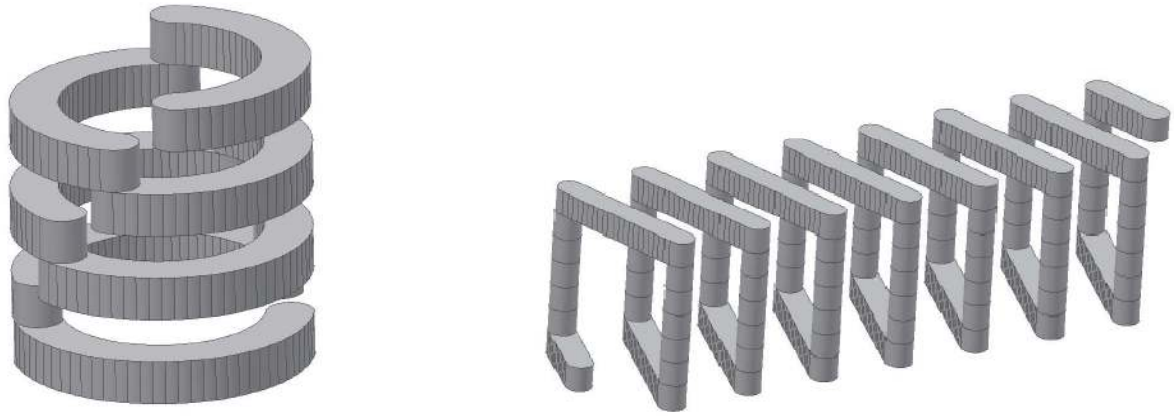
1.2.3 THE SOLUTION?

The solution to this problem, and the subject of this thesis, is to utilize a trace which is significantly thicker than what has been available previously. These thick traces are formed by cutting trenches out of the green tape with a punch and filling them with conductor, much like an oversized and elongated via. Inductors formed this way have been called full tape thickness feature (FTTF), although other names such as Deep Trench have been used for LTCC implementations.

SECTION II - FTTF

2.1 DESCRIPTION OF FTTF

FTTF inductors created with overlapping vias, as illustrated in Figure 2.1, have the potential to have significantly better Q and self-resonant frequency (SRF) than other integrated inductors [5][15]. This is because their turns have a larger surface area and much larger cross-sectional area than inductors made on-chip or from LTCC flat metals. This can help overcome high-frequency non-idealities such as skin effect, current crowding, and proximity effect [3]. Of course, it can still be seamlessly mixed with any amount of traditional flat metal features and surface mount components on the board/system being built.



A B

FIGURE 2.1: VERTICAL(A) AND HORIZONTAL(B) SOLENOIDS CREATED USING OVERLAPPING PUNCHED VIA STRUCTURE IN LTCC MATERIAL

2.2 PERFORMANCE OF FTTF INDUCTORS

As frequency increases, the reactance of an inductor increases linearly. Because Q can be found as X/R_s, we might infer that Q will also continue to increase linearly. Indeed, for low frequencies this is what happens. However, that trend does not continue. Eventually, resistive losses in the inductor begin to increase, and then to overwhelm the linearly increasing reactance. The increase in resistive losses is caused when the effective cross-sectional area of the conductor is decreased. This basic skin effect phenomenon restricts the flow of current to the surface of a conductor. The reduction in usable cross-sectional area increases the resistance of a trace with the square root of frequency. The area containing the current is defined by the skin depth (δ) as shown in Figure 2.2. Because FTTF traces have more surface area, they have lower resistance even when δ is very small.

Edge singularity and proximity effect will also drive current to the outer edge of a trace. Edge singularity is the tendency for a larger portion of a current to migrate to the outer edges of a conducting line. An isolated FTTF line, being close to square, should see a migration to all four faces of the conductor. The effect is similar to skin effect in this sense, but has its own transition frequencies and behaviors [3]. This explains why the internal resistance of a conductor tends to increase somewhat faster than the 1/f that is suggested by skin effect alone.

Proximity effect or current crowding takes place when the tangential magnetic field on a region of any conductor is partially or fully canceled by the magnetic field of one or more additional traces [6]. For a solenoid this means there is going to be a reduced current flowing on the surfaces of the turns which face each other as in Figure 2.3. Because of the B field distribution, there will be little current flow on the top or bottom of the line [7] except at the lines near the inductor ends. The same B field cancelation results in current flowing only on the inside edges of

solenoids. Similar effects occur in planar spiral inductors, although these losses are often dwarfed by losses in the underlying semiconducting substrate which limits Qs to the range of 5 to 20 depending on frequency [2]. Even for inductors in processes like Silicon-on-Sapphire, planar spiral inductors suffer from strong current crowding, resulting in Q values being typically limited to less than 40 in the GHz range and less than 15 at UHF [8][9]. In contrast, the solenoidal structure of FTTF inductors can have Qs up to 100 as shown in this thesis.

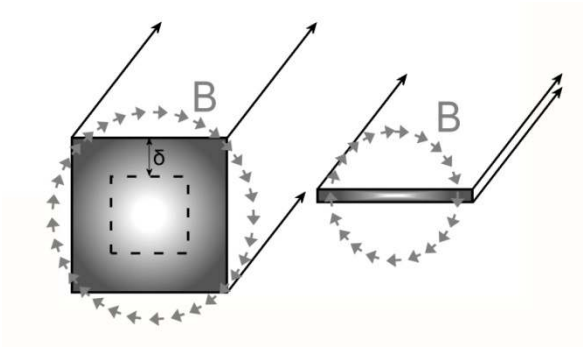


FIGURE 2.2: UNEVEN CURRENT DISTRIBUTION CAUSED BY SKIN-EFFECT. HERE, DARKER SHADING INDICATES A HIGHER CURRENT DENSITY.

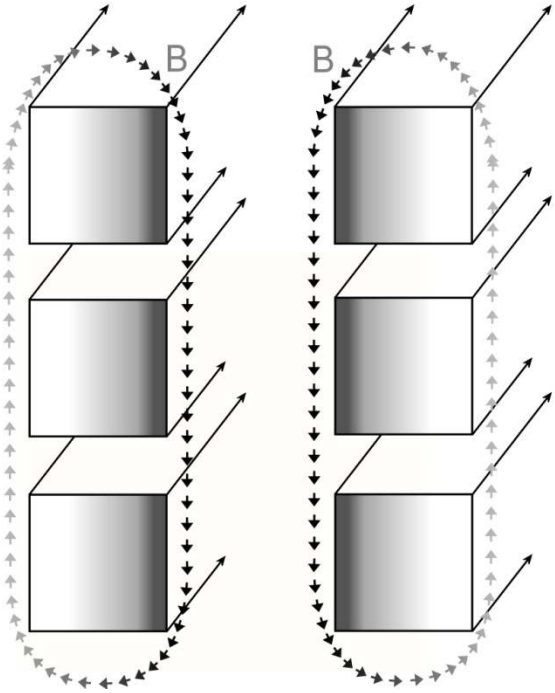


FIGURE 2.3: UNEVEN CURRENT DISTRIBUTION CAUSED BY SKIN EFFECT PLUS PROXIMITY EFFECT IN A SOLENOID.

2.3 TRADEOFFS WITH CLASSIC THIN FILM SPIRALS AND SOLENOIDS

That is not to say that using this method does not have its limitations. There are special design and manufacturing issues to be considered. For example, the large number of punching operations may reduce yield. The problems with bond wire parasitics also remain for components interfaced with active on-chip circuits. Finally, there is a significant cost in time needed for punching out the trenches. For many applications this technology may therefore be cost-prohibitive. It is, however, well-suited to the requirements of high-performance, high-durability applications where LTCC is the substrate of choice.

2.4 DESIGN AND LAYOUT CONSIDERATIONS

When designing a FTTF structure, there are several restrictions to keep in mind. Because the elements span the thickness of the tape, they are 'open' to the layers above and below. This means that they can contact both flat metal printed onto the tape layer as well as other FTTF elements. These will short together if they cross on adjacent layers. For this reason, a layer of tape must be left between each turn of an inductor. Also, the physical stability of the tape must be taken into consideration. To form a FTTF, a significant amount of green tape must be removed by punches. Care must be taken so that a section of tape does not become isolated enough that it can no longer be supported. In other words, if a trench is cut out around an area, then that section of tape will simply fall out. This is the case for a solid ground shield surrounding a structure. To get around this, 'windows' are left in the

shield to provide supporting material for the tape inside the shield. The 'windows' should be staggered between layers in such a way as to allow conduction around them.

An alternative to punch out the vias and trenches one punch at a time, also referred to a 'nibbling', is to utilize lasers for the task. This is actually the more widely applied technique utilized in industrial LTCC applications because it can be accomplished more quickly. It has the added benefit in our case of not physically fatiguing the green tape due to repeated strikes by the punch. However, the equipment to do so is more costly than the punching process and has a shorter lifespan. More importantly, laser cutting has other drawbacks which limit its usefulness in this particular application. The cuts which are made by the beams have rough sides, and the cuts do not have a consistent width for the entire cross-section of the tape [15] as in Figure 2.4.

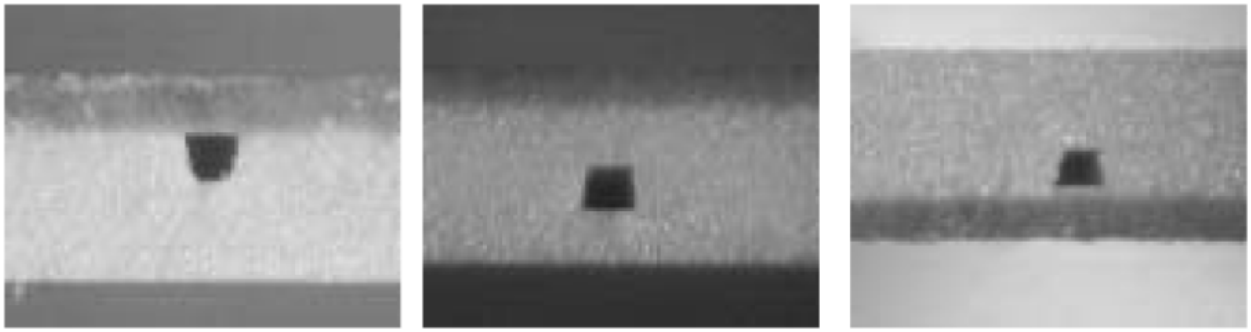


FIGURE 2.4: EXAMPLES OF LASER-CUT VIA CROSS-SECTIONS [15]

SECTION III - INDUCTOR ARRAY

3.1 INDUCTOR DESCRIPTIONS

This research was intended to be very exploratory. To this end, we came up with a wide selection of structures to be fabricated in an array pictured in Figure 3.1. Most of these arrays were then sawed into individual chips like those pictured in Figure 3.2 to minimize coupling effects on measured performance.

The array inductors can be lumped into two main categories: vertical and horizontal. The vertical varieties are oriented with their z-axis, or length, perpendicular to the plane of the array, as in Figure 2.1a. The horizontal varieties have a z-axis parallel to the array, as in Figure 2.1b. Within each category, several varieties are investigated. Varieties are indicated by a letter (A-M) and have several variations where parameters are altered. The pool of parameters we examined are trench width, number of turns, overall inductor diameter, punch overlap, pitch, inductor length, layer spacing, layer connection scheme, and the presence of ground shields. Not every combination of these parameters could have a variation; there would be far too many. Many of these parameters only apply to one or a few of the varieties. A summary of the inductors and other structures created is given in Tables 3.1-3.5 below. ***Images of each inductor variety can be found in the Appendix, along with estimated values of L, Q, and SRF.*** In addition, several special-case geometries were also developed.

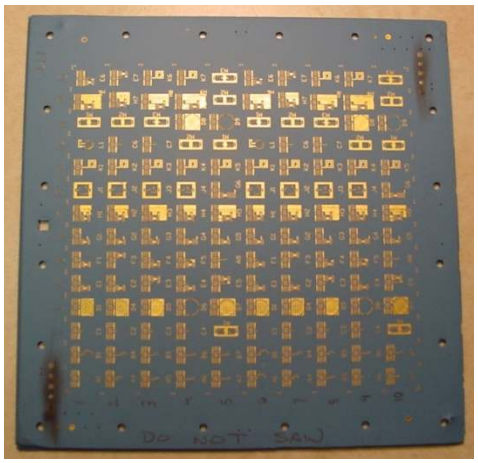


FIGURE 3.1: A PANEL OF THE INDUCTOR ARRAY

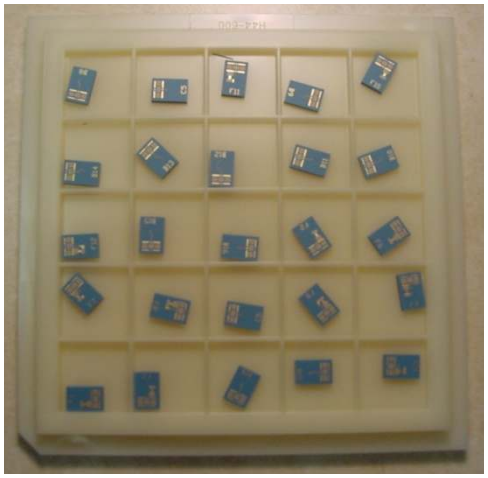


FIGURE 3.2: INDIVIDUAL STRUCTURES AFTER BEING SAWED INTO CHIPS

TABLE 3.1: TYPE A, VERTICAL SOLENOID

Name	Geometry	Est. L	Est. Q(500MHz)	Est. SRF
A1	80mil dia, 7mil punch, 10 layers	52nH	59	1.5GHz
A2	80mil dia, 5mil punch 10 layers			
A3	80mil dia, 12mil punch, 10 layers			
A4	40mil dia, 7mil punch, 15 layers	29nH	47	3.4GHz
A5	20mil dia, 7mil punch, 15 layers	8.4nH	30	8.0GHz
A6	20mil dia, 7mil punch, 10 layers	5.2nH	27	7.9GHz
A7	20mil dia, 7mil punch, 5 layers	2.1nH	23	7.1GHz
A8	10mil dia, 7mil punch, 5 layers	0.6nH	16	13GHz

TABLE 3.2: TYPE B, DOUBLE-THICKNESS SOLENOID

Name	Geometry	Est. L	Est. Q(500MHz)	Est. SRF
B1	80mil dia, 7mil punch, 7 layers	21nH	69	2.7GHz
B2	80mil dia, 5mil punch, 7 layers			
B3	80mil dia, 12mil punch, 7 layers			
B4	40mil dia, 7mil punch, 7 layers	6.7nH	46	6.2GHz
B5	40mil dia, 7mil punch, 3 layers	2.1nH	33	4.3GHz
B6	20mil dia, 7mil punch, 7 layers	1.9nH	30	14GHz
B7	20 mil dia, 7mil punch, 3 layers	6.7nH	24	7.2GHz

TABLE 3.3: TYPE C, FLAT METAL SOLENOID

Name	Geometry	Est. L	Est. Q(500MHz)	Est. SRF
C1	80mil dia, 8 Turns, 1 layer spacing, 10mil wide	164nH	17	1.1GHz
C2	80mil dia, 8 Turns, 2 layer spacing, 10mil wide	110nH	11	1.6GHz
C3	40mil dia, 15 turns, 1 layer spacing, 10mil wide	120nH	13	2.0GHz
C4	40mil dia, 15 turns, 1 layer spacing, 15mil wide	120nH	13	1.6GHz
C5	40mil dia, 15 turns, 1 layer spacing, 10mil wide			
C6	20mil dia, 15 turns, 1 layer spacing, 10mil wide	34nH	7.4	4.9GHz
C7	20mil dia, 15 turns, 1 layer spacing, 15mil wide	34nH	7.4	3.7GHz
C8	20mil dia, 15 layers, 1 layer spacing, 5mil wide			

TABLE 3.4: TYPE D, VERTICAL SOLENOID W/ CAGE

Name	Geometry
D1	80mil dia, patterned, 7mil punch
D2	80mil dia, patterned, 5mil punch
D3	80mil dia, patterned, 12mil punch
D4	40mil dia, patterned, 7mil punch
D5	40mil dia, solid, 7mil punch
D6	40mil dia, open, 7mil punch
D7	20mil dia, patterned, 7mil punch
D8	20mil dia, solid, 7mil punch
D9	20mil dia, open, 7mil punch

TABLE 3.5: TYPE E, DOUBLE LAYER SOLENOID

Name	Geometry
E1	80mil/50mil dia, 15 layers
E2	80mil/40mil dia, 10 layers
E3	80mil/50mil dia, 15 layers
E4	80mil/50mil dia, 5 layers
E5	50mil/20mil dia, 15 layers
E6	50mil/20mil dia, 10layers
E7	50mil/20mil dia, 5 layers

TABLE 3.6: TYPE F, DOUBLE-THICKNESS, DOUBLE-LAYER SOLENOID

Name	Geometry
F1	80mil/50mil dia, 7 layers, 7mil punch
F2	80mil.50mil dia, 7 layers, 10mil punch
F3	80mil/50mil dia, 3 layers, 7mil punch
F4	50mil/20mil dia, 7 layers, 7mil punch
F5	50mil/20mil dia, 3 layers, 7mil punch

TABLE 3.7: TYPE G, HORIZONTAL SOLENOID

Name	Geometry
G1	3 turns, 12mil pitch
G2	6 turns, 12 mil pitch
G3	3 turns, 18mil pitch
G4	6 turns, 18 mil pitch
G5	3 turns, 24mil pitch
G6	6 turns, 24 mil pitch

TABLE 3.8: TYPE H, HORIZONTAL SOLENOID WITH CAGE

Name	Geometry
H1	3 turns, 12mil pitch, .5dia shield width, 1dia shield length
H2	6 turns, 12mil pitch, .5dia shield width, 1dia shield length
H3	6 turns, 12mil pitch, 1dia shield width, 2dia shield length
H4	3 turns, 18mil pitch, .5dia shield width, 1dia shield length
H5	6 turns, 18mil pitch, .5dia shield width, 1dia shield length
H6	6 turns, 18mil pitch, 1dia shield width, 2dia shield length
H7	3 turns, 24mil pitch, .5dia shield width, 1dia shield length
H8	6 turns, 24mil pitch, .5dia shield width, 1dia shield length
H9	6 turns, 24mil pitch, 1 dia shield width, 2dia shield length

TABLE 3.9: TYPE K, FLAT SPIRALS

Name	Geometry
K1	15 layers, series
K2	5 layers, series
K3	1 layer (Single Spiral)
K4	15 layers, parallel
K5	5 layers, parallel
K6	15 layers, stacked
K7	5 layers, stacked

3.2 INITIAL L & Q ESTIMATIONS

It is straightforward to make estimations of some of the more basic varieties. However, these estimates are made using several approximations. They assume perfect alignment of the tape layers and reasonable approximations of surface current distribution. To estimate L, the Wheeler formula for single-layer solenoids [10] is used:

$$L = \frac{N^2 r^2}{9r + 10LEN} \tag{1}$$

where *L* is inductance in µH, *N* is the number of turns, *r* is the radius in inches, and *LEN* is the length of the coil in inches. This formula is applied to the vertical varieties as well as the horizontal which are not round as the formula assumes.

To estimate inductor Q, the resistance of the inductor turns must be found. Each of the inductors has a frequency-dependent internal resistance. These equations are on the inductor geometries and conductor properties. The conductor is assumed to be reduced to only the area carrying current as determined by one skin depth δ [11] on the inside of the coil as follows:

$$R = \frac{l_{path}}{\sigma A} \tag{2}$$

The cross sectional area of the vertical inductors, A_{vert}, can be approximated as

$$A_{vert} \cong \delta h \tag{3}$$

where δ is skin depth and σ is conductivity of the fired gold paste (σ=2.22E7 s/m in our case), and *h* is the thickness of the traces corresponding to the tape thickness. The cross sectional area of the horizontal inductors, A_{horiz}, can be approximated as one of two values. One is for the region of each turn which is parallel to and lies entirely within a single layer of tape. The other is for the region of each turn which is normal to the tape layers and can be thought of as a stack of individual via punches. Every turn is in each of these two regions for an equal length.

$$A_{horiz} \cong w\delta \quad \text{or} \quad A_{horiz} \cong \frac{\pi w \delta}{2} \tag{4}$$

where *w* is the width of the traces corresponding to the punch diameter. l_{vert} and l_{horiz} are the path lengths of the vertical and horizontal inductors, respectively. This is the distance the conductor would cover if it could be straightened.

$$l_{vert} = 2\pi r N \qquad l_{horiz} = (4N)(2r) \tag{5}$$

The AC resistance of the coils can be found by substituting (4) and (5) into (3).

$$R_{vert} \cong \frac{2\pi rN}{\delta h \sigma} \qquad R_{horiz} \cong \frac{4Nr}{w\delta\sigma}\left[1+\frac{2}{\pi}\right] \tag{6}$$

Finally, the Q factor is found by the well-known equation

$$Q = \frac{2\pi fL}{R} \tag{7}$$

All dimensions are in meters, including *r* and *l*. This does not account for the extra current-carrying area on the top and bottom turns and so the approximations can be considered conservative estimates. They only apply for frequencies where 2δ<w.

3.3 Self Resonant Frequency Estimations

The internal capacitance that sets the self-resonant-frequency (SRF) is approximated as only being contributed by the conductor area directly between two turns. This approximation can be considered optimistic, since it ignores sidewall fringing fields, and is therefore not appropriate for simulation work. However, it is sufficient to guide development of the test array. The basic formula for 2-plate capacitance which approximates a single turn is

$$C = \frac{\varepsilon A}{d} \tag{8}$$

Where ε is the permittivity of the dielectric (in this case it is the LTCC substrate), A is the area between two parallel plates, and d is the distance between those plates. In the case of the vertical inductors, *A* is approximated to be the area of a ring defined by the radius and trace width. They are separated by one tape thickness. To find the total internal capacitance, this value is divided by the total number of inter-turn gaps.

$$C_{vert} = \frac{\pi((r+w)^2-r^2)\varepsilon}{h}\frac{1}{(N-1)} \tag{9}$$

In the case of the horizontal inductors, *A* can be considered to be the sum capacitance between the horizontal and vertical members. There are two sets of each for every turn and they are of length 2*r*. Here, the gap distance is *pitch*-*w*. Again, to find the total internal capacitance, the value is divided by the total number of inter-turn gaps.

$$C_{horiz} = \frac{\varepsilon(2h+\pi w)2r}{(pitch-w)}\frac{1}{(N-1)} \tag{10}$$

where *pitch* is the spacing between trace centers in the case of the horizontal inductor. This does not account for any capacitance to any shield, vias, or probing structures. Finally, the SRF was estimated as,

$$SRF = \frac{1}{2\pi\sqrt{LC}} \tag{11}$$

Several varieties of inductors shown in Section 3 have no estimations. This is because their complicated structures make forming accurate estimations difficult and outside the scope of this work.

SECTION IV - MEASUREMENTS

Measurements were taken with an HP8735E Network analyzer and GGB Industries ECP18-GSG-500-DP coplanar probes, pictured in Figure 4.1. The measurement system was calibrated using a GGB CS-9 calibration substrate.

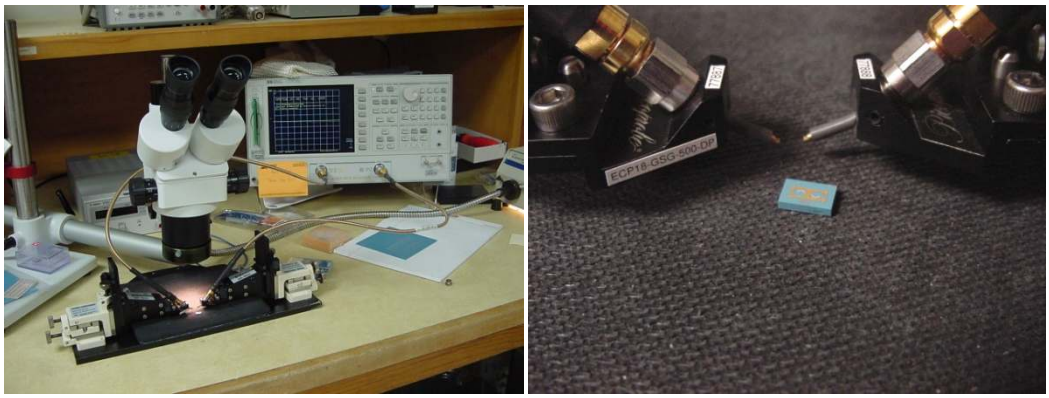


FIGURE 4.1: TEST BENCH

4.1 ISSUES WITH HIGH-Q MEASUREMENTS

Since expected Q values for some structures in the array may reach 100 or more, high accuracy is essential. To illustrate this point, example measured results are shown in Figure 4.2.

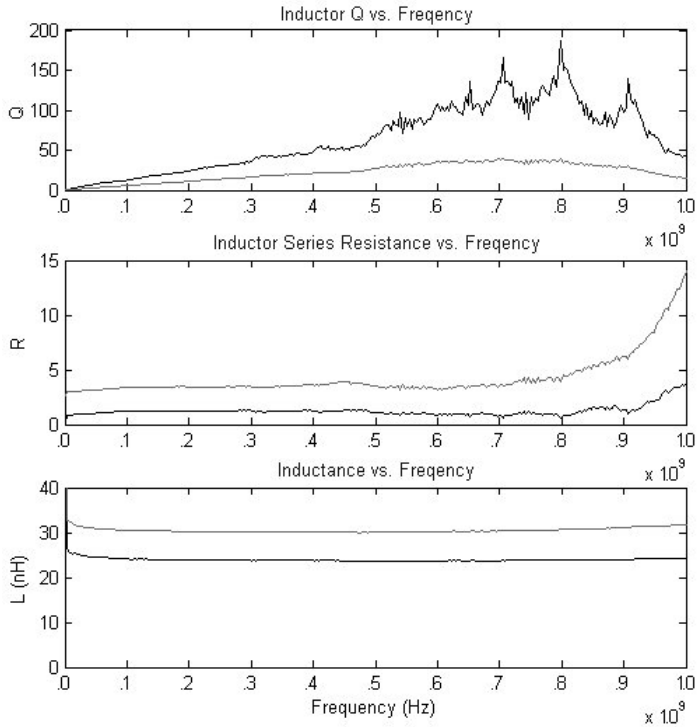


FIGURE 4.2: A SAMPLE OF TWO MEASURED INDUCTORS WHERE ONE INDUCTOR HAS A |Γ| NEAR 1.

In Figure 4.2, the curves themselves hint at the problem, which is virtually always overlooked in the reported literature, Reported curves are often smoothed by curve fitting to models, or are simply (and deceptively) smooth from the beginning. A network analyzer has very real limitations on its accuracy in measuring both the magnitude

and angle of gamma, which make the measured values also subject to significant accuracy limitations – especially when measuring impedances near the outer boundary of the Smith Chart. For example, consider the case of an inductor with an impedance value of jZ_0+R_S. As stated previously, Q is defined as the ratio between the real and imaginary components of the impedance. Hence, Q is simply Z_0/R_S in this example.

$$Q = \frac{IM\{Z\}}{RE\{Z\}} = \frac{Z_0}{R_S} \tag{12}$$

However, the network analyzer measures Γ values rather than R and X values. In terms of Γ, for this inductor we can write:

$$Q = \frac{IM\left\{Z_0\frac{1+j|\Gamma|}{1-j|\Gamma|}\right\}}{RE\left\{Z_0\frac{1+j|\Gamma|}{1-j|\Gamma|}\right\}} = \frac{2|\Gamma|}{1-|\Gamma|^2} \tag{13}$$

Solving for |Γ| in terms of Q,

$$|\Gamma| = 1 - \frac{1}{Q}. \tag{14}$$

Q(Γ) is plotted in Fig. 4.3 From this graph, it is clear that an accuracy of better than 1% is required to measure a Q of 100. For example, if a gamma magnitude accuracy of 0.5% is assumed, the displayed Z for an inductor with an actual Q of 100 can imply a Q anywhere from 66 to 200.

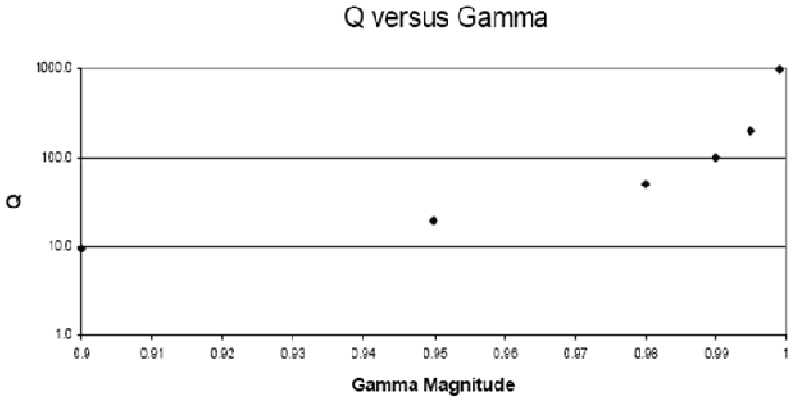


FIGURE 4.3: Q VERSUS GAMMA FOR BEST CASE MEASUREMENT (ANGLE GAMMA = 90 DEGREES)

Figure 4.4 shows the HP8753E's specified gamma measurement accuracy after use of a high-quality calibration standard. Clearly the raw accuracy of the HP8753E is insufficient to quote even a single significant digit in the range of Q=100. This could explain the 'noisy' appearance of the Q measurements above 80 in the case of the vertical inductor. This issue of Q measurement accuracy was a major concern near the start of this project. However, the inductors had generally lower Qs than initially expected. This made the question of Γ accuracy less significant than it could have been. Further developments could lead to measurements of higher-Q structures that should be carefully considered before reporting Qs in the neighborhood of 50 and above.

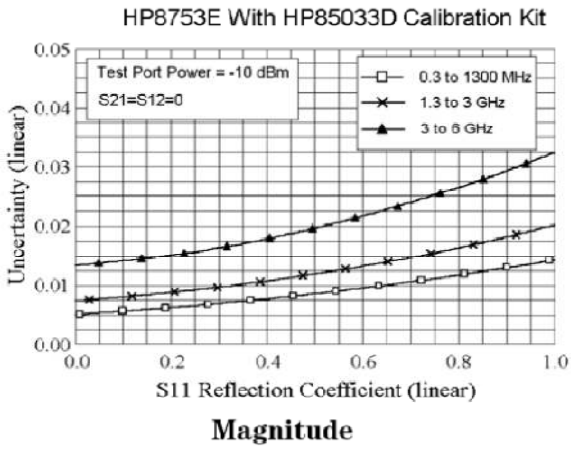


FIGURE 4.4: HP/AGILENT DATASHEET GRAPH OF SPECIFIED GAMMA MAGNITUDE ACCURACY (FROM AGILENT WEBSITE)

4.2 MEASUREMENT SOLUTIONS

There are many ways to overcome these measurement issues. To start with, careful calibration is critical. Using a 2-port approach can help give more accurate results [12], but there is a limit to hardware sensitivity. Without access to more sensitive (and expensive) equipment there are ways to boost the accuracy of a measurement at the cost of physical or computational complexity. Four methods were chosen to be applied to this study to provide validation of the high Q results expected.

4.2.1 DIRECT S11

This measurement technique has the advantage of simplicity. It also allows for simple and accurate measurement of L and SRF. One end of an inductor is connected to ground so the inductor becomes a simple one-port device with Γ=s11. The Q can be found from the magnitude and angle of Γ. The SRF can be found directly from the frequency where angle of Γ becomes greater than 180°. The L value can be easily found at low frequencies. This measurement requires no external components and so can have a very minimal probing structure. However as mentioned previously, it produces questionable results for Q when Q exceeds about 100.

4.2.2 SERIES RESONANT / PARALLEL RESONANT

When calibrating a VNA with the classic method used at low frequencies (<2GHz), measurements are taken of an 'ideal' short circuit, an open circuit, and a 50Ω load. It then stands to reason that these points should be the most accurately calibrated and, therefore, the most accurate points for measurement as well. The series resonant method uses this idea by using an external capacitor placed in series with the inductor to, at a chosen frequency, create a short circuit while preserving the same internal series resistance as it would have if were not part of a resonator. Q can then be found from X/R_s where X is derived from the previously measured L value and the frequency. The parallel resonant method is similar. It uses a capacitance in parallel with the inductor to create an open circuit at a chosen frequency. This method preserves the parallel resistance rather than the series resistance. Q can then be found from R_p/X.

Using these methods introduces some new problems. External components are not easily tuned, making it difficult to get a measurement at a specific frequency. The caps also must be assumed to be ideal; their internal resistances need to be small enough that those of the inductor swamp them. This can be a problem at RF and requires the use of RF caps. They also need to be connected to the inductor, which is buried in ceramic. Pads must be added to the probing structure. These can be quite large In comparison to the DUT. Due to the need to keep all connections physically short, they must be located very close to the inductor. It is possible that these large

metal surfaces could have a detrimental effect on the net performance. A good connection between the two requires the use of solder. This too is a problem because solder dissolves gold. Fortunately, the LTCC fabrication process used allows for gold on the top and bottom surfaces to be covered in a platinum paste which is solderable and protects the pads below it.

4.2.3 2-PORT RESONANT

This method makes use of the property of filters that says

$$Q = \frac{f_0}{BW} \tag{15}$$

Q can then be found by implementing the inductor in a filter. If the capacitor used to form the filter's resonator has a small resistance in comparison to the inductor and the source and load impedances are properly considered, the Q of the filter can be approximated to be the Q of the inductor [13]. The filter formed in this case can be band pass or band stop. However, a band pass filter would require additional decoupling caps at the input and output to keep the VNA from loading the filter. A band stop filter such as the one shown in Figure 4.5 requires no additional components other than the resonating cap. This is the technique we view as producing the most accurate results. It is not an ideal solution as it has many of the same drawbacks as the series/parallel resonant techniques; the need for external components and the large pads to support them are examples. Also, for each cap applied, the Q can be measured at only one frequency. It is not feasible to collect data at many frequencies. This reduces the usefulness of the 2 port method. However, for our purposes, it provides a single point frequency validation of results from the other techniques.

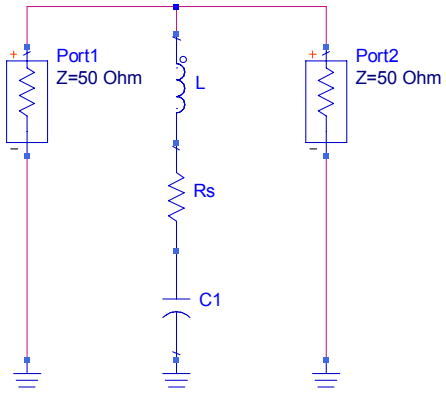


FIGURE 4.5: 2-PORT MEASUREMENT SETUP

The measurement technique discussed in [13] shows that the unloaded Q can be found from the attenuation, A_{dB}, of the filter rather than the BW as:

$$Q = \frac{4\pi f L}{Z}\left(10^{\frac{A_{dB}}{20}} - 1\right) \tag{16}$$

This equation agrees well with the BW method, and provides results which are similar to the one found from the BW. It is less convenient to use because it requires knowledge of the inductance value which must be obtained from the direct S11 measurement. The need for an additional measurement could also introduce unnecessary error. For this reason, we chose not to utilize it.

4.3 GAMMA CORRECTION

Direct S11 measurement would be the best option for gathering the data on Q for a large set of frequencies if it could be 'perfectly' calibrated. No calibration is ever going to be perfect, but the errors in a particular calibration will be consistent from measurement to measurement if temperature and other factors are carefully controlled. If the error can be found using a suitable reference standard, then it can be corrected. We call this post-measurement data processing "gamma correction". It uses a microstrip line which can be produced to have a very specific inductance. A microstrip line is simple to accurately simulate. The VNA is used to measure both the DUT and line. The gamma at each frequency point of the line is compared to its simulated value. This represents the error in the calibration/VNA at that particular frequency. This is then used to correct each point of the DUT. Preliminary experimentation indicates that this is likely to work, if certain obstacles can be overcome. The most significant of these is the need for a microstrip line of a specific inductance for every unique structure, such as those in Figure 4.6.

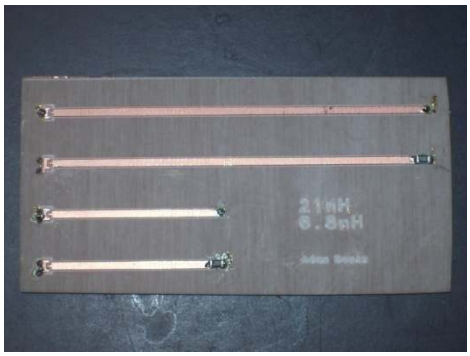


FIGURE 4.6: MICROSTRIP LINE USED FOR GAMMA CORRECTION

To test the feasibility of this idea, the following experiment was conducted. The first step was to simulate the gamma response of a microstrip line. The fabricated line was measured and a correction factor was found by comparing the measurement to the simulation. This was then applied back to the microstrip measurement and an output close to the simulation resulted as in Figure 4.7. The result is not exactly like the simulation, but it is very similar. This is to be expected because the correction factor was created from this line.

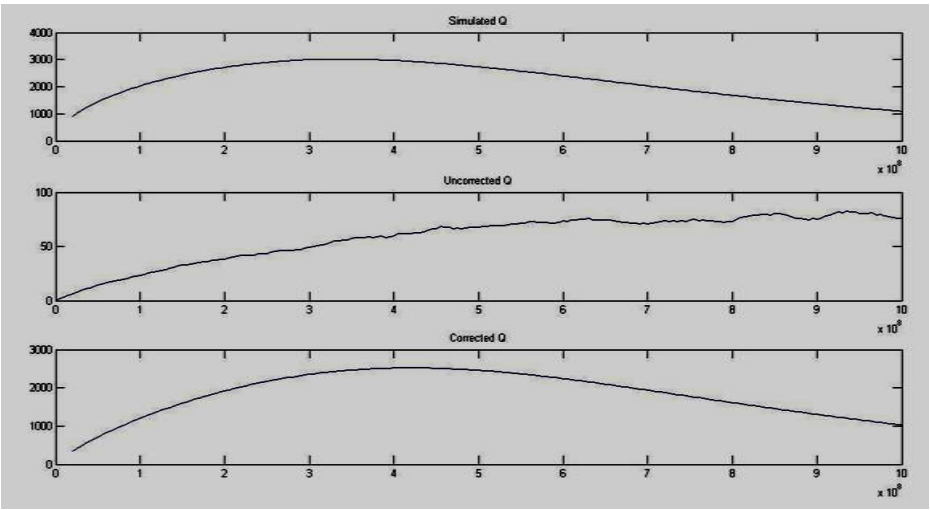


FIGURE 4.7: GAMMA CORRECTION APPLIED BACK TO THE MICROSTRIP LINE IT WAS CREATED FROM

The next step was to measure an inductor. For this test we used a Coilcraft 0805HQ chip inductor. As shown in Figures 4.8 and 4.9, the uncorrected measurements are much improved when the gamma correction is applied to them. However, further investigation will be required to confirm the reliability and accuracy of this technique.

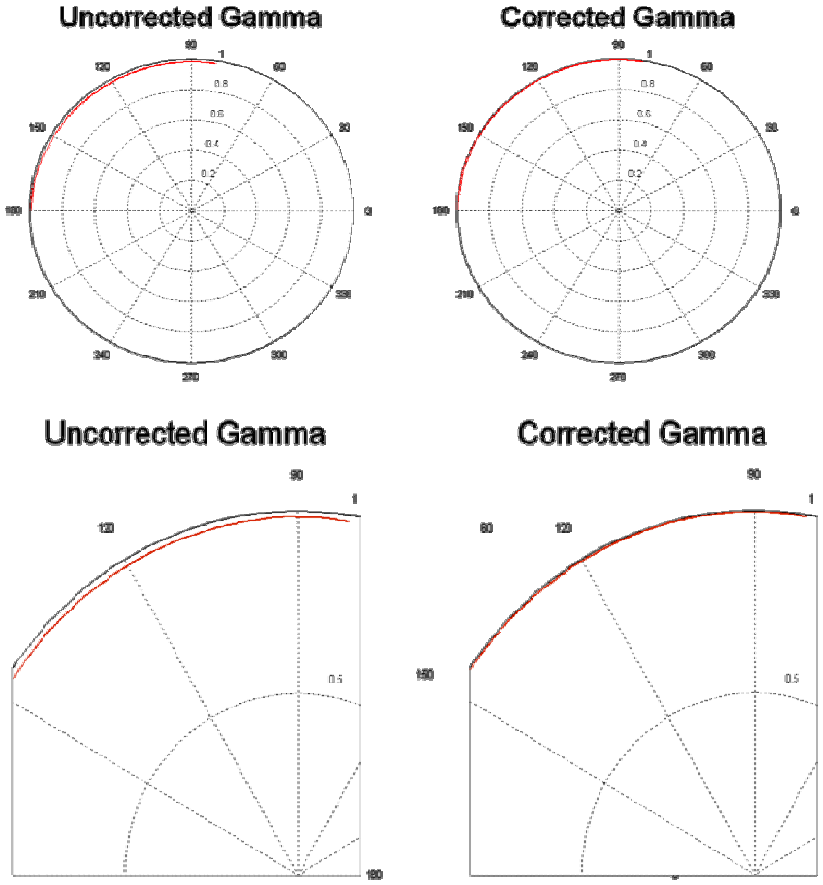


FIGURE 4.8: MEASURED GAMMA BEFORE AND AFTER CORRECTION

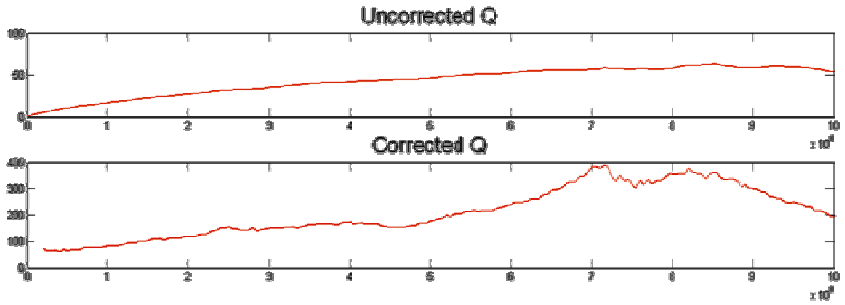
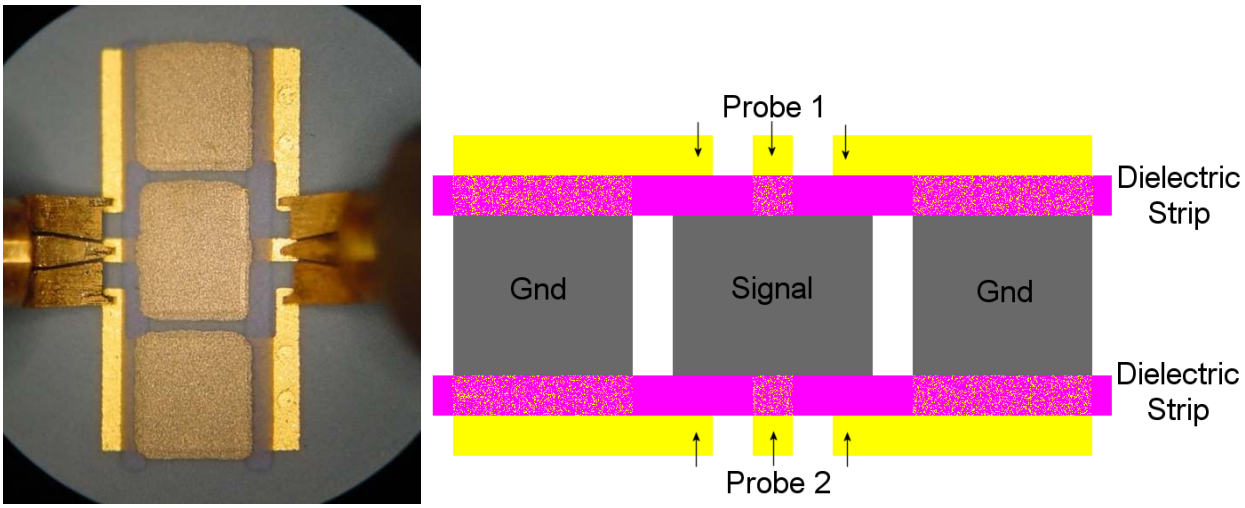


FIGURE 4.9: GAMMA CORRECTION Q PLOTS

4.4 PROBING STRUCTURE

To make fabrication easier, we developed a probing structure which can facilitate all of the measurement techniques previously mentioned. The structure consists of a set of probe pads, space for two parallel caps, space for one series cap, and all the vias and traces which are not part of the inductor structure but are necessary to tie the parts of the probing structure together. All of the probe pads and parallel caps are on the top surface layer of the LTCC (See Figure 4.10). Most of the series caps go on the bottom surface layer, but some are on the top (See

Figures 4.11, 4.12). This arrangement was chosen to balance the need for versatility against the need to keep all ancillary elements as short and minimal as possible.



a b

FIGURE 4.10: TOP SIDE PROBING STRUCTURE W/O CAPS

FIGURE 4.11: BACK SIDE SERIES CAP PAD

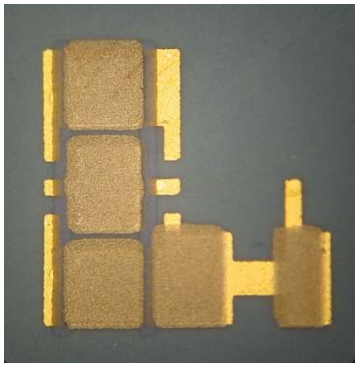


FIGURE 4.12: PROBING STRUCTURE WITH TOP SIDE SERIES CAP PAD

The series cap is initially shorted by a section of gold between its platinum-plated pads. This allows direct s11 and then the parallel resonant measurements to be taken unhindered. Once the parallel caps are removed, the short across the series cap pads can be easily removed by dissolving the gold in a solder bead. Series resonant and 2 port resonant measurements can then be taken. To keep solder from damaging the probes contacts points, stripes of dielectric material were laid down between the solder pads and the contact points as in Figure 4.10b. These strips act like a solder mask and help contain the solder flow.

SECTION V - RESULTS

The following results presented in Table 5.1 were taken from direct S11 measurements. The numbers were determined by mathematically removing the effects of internal capacitance. This shunt capacitance is determined from the L and SRF. Removing its effects allows for a Q to be measured based on the "energy stored/energy dissipated" definition, rather than the X/R definition [14].

5.1 BY VARIETY

TABLE 5.1: S11 MEASUREMENT RESULTS

	L(nH)	SRF(GHz)	Qmax	f(Qmax)
A1	50	0.736	63	0.52
A4	28	1.15	50	0.66
A5	10	2.25	36	0.848
A6	8	2.58	36	1.23
A7	5	3.2	38	2.81
A8	6	3.57	32	2.83
B1	20	1.17	63	0.663
B4	9	2.23	46	0.845
B5	5	3.23	41	2.81
B6	6	3.13	36	0.951
B7	4	3.81	40	2.68
C1	135	0.444	45	0.298
C2	100	0.537	42	0.298
C3	120	0.56	34	0.552
C4	120	0.54	32	0.528
C6	41	1.11	23	0.803
C7	44	1.01	23	0.799
D1	41	0.532	32	0.512
D4	18	0.952	37	0.803
D5	15	1.07	34	0.919
D6	19	1.17	50	1.17
D7	8	1.78	35	1.73
D8	8	1.86	36	0.173
D9	9	2.31	43	2.24

	L(nH)	SRF(GHz)	Qmax	f(Qmax)
E1	62	0.555	43	0.307
E2	52	0.659	44	0.533
E3	11	0.731	42	0.562
E4	18	1.3	45	0.812
E5	34	0.81	30	0.651
E6	24	1.13	33	0.813
E7	7	2.71	27	1.37
F1	29	0.842	50	0.52
F3	10	1.7	42	0.861
F4	13	1.65	34	0.82
F5	5	3.64	28	2.82
G3	10	2.19	34	0.826
G4	19	1.42	41	0.82
G5	10	2.32	42	0.832
H1	5	2.17	30	1.74
H3	16	1.05	43	0.916
H4	9	1.59	40	1.45
H5	16	0.947	39	0.81
K1	550	0.241	11	0.202
K2	72	0.688	25	0.522
K3	10	2.28	40	0.926
K4	6	2.55	28	0.848
K5	6	2.47	35	0.848
K6	6	2.59	27	0.851
K7	7	2.44	33	0.845

Overall, most of the Qs found in Table 5.1 are between 30 and 45. It appears that the inductors with the highest Qs are the simplest structures; the basic A1 and B1 inductors. These are vertical solenoids with an internal diameter of 80mils. The Q plots of all these measurements can be found in the appendix, as well as images of each variety. K1 had the largest inductance value by far; this is not surprising because it has a larger number of turns. The Q of K1 is comparable to what might be found on a silicon IC.

5.2 SELECTED S21

While the probing structure was designed to accommodate all four measurement methods previously mentioned, only direct S11 was employed across the entire array. It would be very time consuming to solder series capacitors to every structure. It would be far more time consuming to solder the parallel capacitors; they are more difficult because there are two caps and they share the 'signal' pad. More importantly, the more complex resonance-based methods were not as important to measurement accuracy as was initially anticipated. This is because, in general, the inductor Qs were not high enough to cause |Γ| to approach 1. The results measured from direct S11 can be assumed to be sufficiently accurate.

To confirm this, we have included 2-port resonant results for **A1** and **B1**, which were estimated and measured to be the highest-Q inductors in the array (See Figures 5.1 and 5.2). Inductor **A1** presented bandwidths of about 11MHz at frequencies around 500MHz (depending on the true value of the external chip capacitor used). This corresponds to a Q of 50. Inductor **B1** presented bandwidths of about 9.6MHz at frequencies around 500MHz. This corresponds to a Q of 52. The results of this measurement do not seem similar to the results of the s11 presented in Table 5.1, but they are taken at different frequencies. Looking at the Q plots in the appendix (*see pages 31 and 33*). you can see that the results agree for **B1**. The plot for suggests that **A1** should be about 60. However, the curve after 400MHz is not smooth. This indicates that this plot may not be reliable.

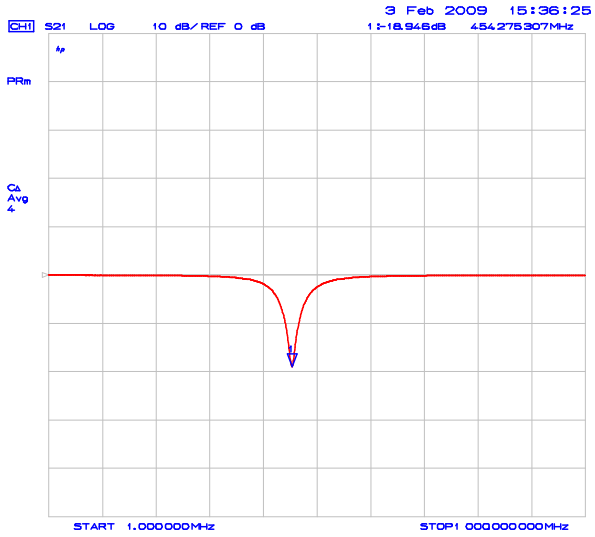


FIGURE 5.1: A1 S21

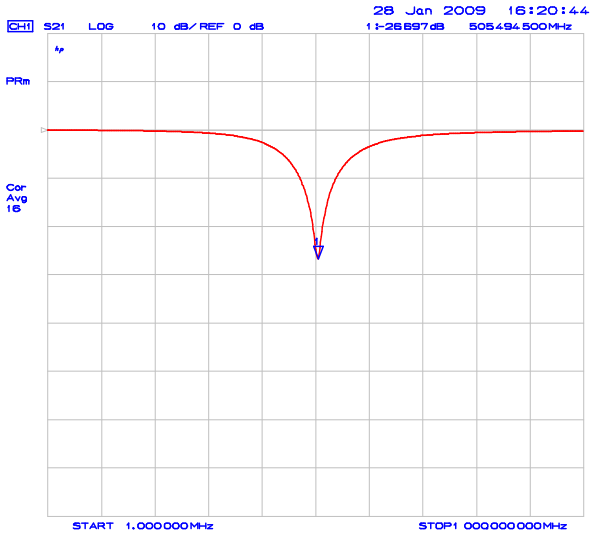


FIGURE 5.2: B1 S21

5.3 COMPARISON OF MEASUREMENT TECHNIQUES

The multiple measurement techniques employed did not prove to be exceptionally helpful. For example, a set of several different copies of **B1** were measured with all four techniques and are shown in Table 5.2. The inductance values are mostly consistent, as this was measured at only 10MHz. The direct s11 measurement gave fairly consistent values. The series s11 resonant method is less consistent, and the parallel s11 resonant method is even less consistent. These variations in measured Q could be attributed to variations in manufacture. Alternatively, they could reflect imperfections and variations in the use of the surface mount capacitor, which were installed by hand. This would make sense because the parallel resonant method used two caps which share a single pad (the 'Signal' pad in Figure 4.10b). These were difficult to mount in a consistent manner. The two-port resonant method gave the highest and most consistent results for Q.

TABLE 5.2: COPIES OF B1 MEASURED WITH DIFFERENT TECHNIQUES

Copy	L (nH)	SRF (GHz)	Direct s11	Series Resonant	Parallel Resonant	Two-Port Resonant
#1	20.8	1.14	48.0	52.2	40.1	52.1
#2	21.8	1.06	42.8	44.2	36.6	51.9
#3	20.7	1.14	49.9	52.1	40.8	53.2
#4	20.7	1.13	50.1	50.7	41.0	51.9
#5	20.5	1.14	48.7	53.7	40.1	50.6
#6	20.5	1.13	47.3	44.9	39.5	48.8

Additionally, these tests were carried out on a couple of lower-Q structures, **A4** and **K3**. **A4** is notable because it is very similar to the inductor used in the 2-pole filter discussed later in Section 7.2. **K3** is a single-layer, two-turn spiral inductor, similar to what might be typically used in LTCC systems. For these, the spread in Q values are not as large between measurement techniques ***or*** between copies. (with the exclusion of **A4** #2 which appears to be an outlier). This holds with the idea that accuracy rapidly deteriorates as $\Gamma \rightarrow 1$. For these inductors, the VNA has sufficient gamma accuracy to rely on the direct s11 measurement.

TABLE 5.3: COPIES OF A4 MEASURED WITH DIFFERENT TECHNIQUES

Copy	L (nH)	SRF (GHz)	Direct s11	Series Resonant	Parallel Resonant	Two-Port Resonant
#1	32.5	>1GHz	35.8	55.2	38.6	45.8
#2	18.3	"	32.5	29.4	16.3	25.5
#3	34.2	"	35.0	54.7	34.8	44.6
#4	34.0	"	35.7	40.4	34.4	45.3
#5	33.8	"	35.6	55.6	37.0	45.4

TABLE 5.4: COPIES OF K3 MEASURED WITH DIFFERENT TECHNIQUES

Copy	L (nH)	SRF (GHz)	Direct s11	Series Resonant	Parallel Resonant	Two-Port Resonant
#1	10.2	>2GHz	30.5	-	-	31.1
#2	10.2	"	30.6	-	-	32.7
#3	10.1	"	30.0	-	-	30.9
#4	10.2	"	29.5	-	-	29.8
#5	10.5	"	28.0	-	-	28.1
#6	10.5	"	29.4	-	-	31.2

SECTION VI - ANALYSIS

In general, measured Q results did not live up to our initial estimates. During the entire process the estimates were continually revised to reflect a better understanding of the behavior of these solenoids and the properties of the materials used to construct them. This is not to say that the results are disappointing; they confirm the general behaviors we expected to see. For instance, the Wheeler formula [10] proved to be a good estimator of the inductance. The Q was shown to be less dependent on the cross-sectional area of the conductor and more dependent on the dimension of the conductor parallel to the axis of the solenoid. It is also possible that the probing structure with its large capacitor pads is deforming or otherwise interfering with the magnetic field of the inductor. The position of the probes was another factor which was noted to impact the measured Q. When the second probe is in use, it must pass directly over the center of the inductor. The 1-port measurements do not require this probe, but if it is left in place (only lifted) there is a visible impact compared to when it is moved away entirely. It stands to reason that the probe's location impacts the 2-port measurement as well, and could be depressing the actual results. This effect has not been quantified but it has been observed.

6.1 YIELD

We have found that process variation is not something which can be neglected. Yield, especially among the more intricate structures, was an issue. Since all failures were open circuits, this could be caused by problems with punching, misaligned tape layers, damaged tape layers, or unfilled trenches.

If the fabrication really did suffer from inaccurate punching, all yield problems could be reasonably blamed on that. However, this is not likely to be the source of the errors. The punching process has a very fine tolerance (perhaps as fine as .1mil). Misaligned tape layers are one likely cause. The because of the human interaction with the alignment process, this has can have errors of up to 2mil. For example, the yield for the 'G' and 'H' type structures (See Appendix) was almost zero. These rely on multiple stacks of 6mil punches. If there is a net misalignment of 6mil, the inductor will be an open circuit. This is not so much of a danger with the other structures. They have small portions of larger features overlapping. If two layers are not perfectly aligned then there is a good chance that parts of the features will still be in contact. Even if poor alignment does not cause an open circuit it can still increase internal resistance and reduce Q.

Damage to the tape layers can happen when a region has too much green tape removed. The tape could tear or sag. This was a major concern with any structure using a shield. 'Windows' were left in the shield to support the tape in the middle, but that may not have been enough. All of these structures had a low yield. In hindsight, a solid ground shield is no more effective than a fence-style shield and probably much easier to fabricate.

Trenches that are not filled was the only visible fabrication problem. As Figure 6.1 shows, some of the open circuit inductors are quite obvious. In these, the metal paste that fills via holes and trenches punched into the tape was not properly distributed or, more likely, crumbled and fell out sometime after firing. The solution to the latter case is simple; FTTFs should be covered with a top layer of tape or flat metal to protect and seal in the metal. Of course, if the trenches were never filled in the first place, this is a problem which could exist on the internal layers as well. In that case the solution would not be so simple.

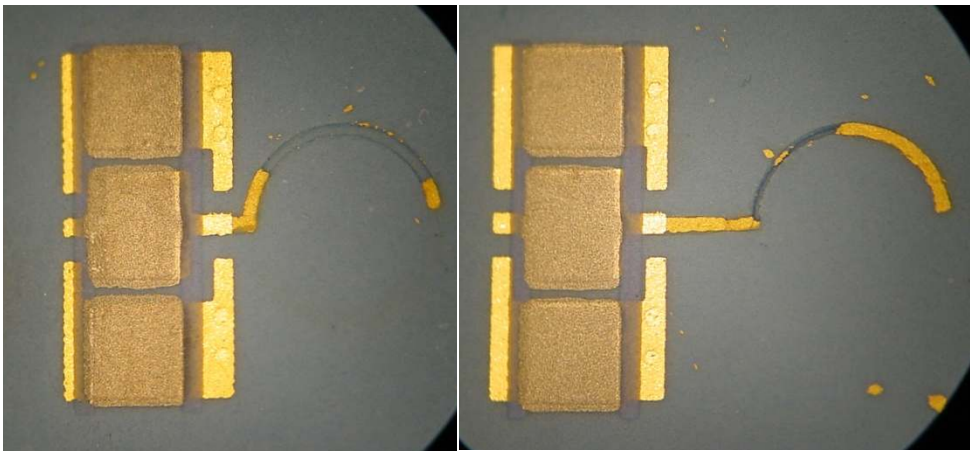


FIGURE 6.1: EXAMPLES OF UNFILLED TRENCHES ON TOP LAYER

Finally, it is possible that the individual layers are forming bubbles or delaminating where the traces contact. It is difficult to know exactly where the true problem lies without performing a failure analysis. This would entail slicing the chips and seeing where the open circuit is occurring. We do not have the capability to perform such a test here at K-State; it will need to be done elsewhere. Knowing for certain what is causing the faults will be very helpful in preventing them in future uses of this technique.

6.2 POSSIBLE IMPROVEMENTS

As we have come to better understand the obstacle which must be overcome to obtain even higher Qs, it has become apparent that the dimension of the conductor parallel to the axis of the solenoid is the key to higher Qs. In the case of the vertical inductors, increasing this dimension corresponds to using a thicker tape. SRF can be maximized by limiting the surface area between the turns of the coils. Decreasing this corresponds to using a smaller punch size to cut the trenches for the features. There are, of course, limiting factors that must be taken into account. A rule of thumb for LTCC punches is that

$$\frac{diameter_{punch}}{thickness_{tape}} \geq 1$$

It should be possible to 'double' up multiple thin tape layers allowing the use of a smaller punch, much like was done in varieties '**B**' and '**F**'. In this case, the tradeoff is complexity of tape alignment. Another tradeoff when using thicker conductors is a reduction in the total possible number of turns for a single inductor. It would have been helpful to have seen how the inductors would have performed.

The ground shields remain an open issue. The scope of this thesis does not include measuring the effectiveness of the shields at isolating the inductors from outside interference. They do, however, have a negative impact on yield. This was the major concern with the shields since the decision was made to include them in the array. For best yield, a picket fence-style of shield (using vertical vias connected by rings of flat metal) may be just as effective as our nearly-solid walls of metal.

SECTION VII - ADDITIONAL STRUCTURES

Along with the array of inductors, some unique structures were prototyped. Without results from the inductors, these are intended to lay the groundwork for the more complicated (and useful) structures which could most benefit from this concept.

7.1 DEEP LOOP RESONATOR

The deep loop resonator pictured in Figure 7.1 is descriptively named. It is an 80mil-diameter, single-turn inductor with a vertical axis which is 15 tape layers thick. Interspersed between the ends of the loop are the plates of a parallel capacitor, making this a resonator. The purpose of this structure is to examine what happens when the features which make something high-Q are carried to an extreme. The estimations applied to the other inductors suggest a Q of up to 300. This structure has

a) Very thick traces
b) A very large diameter
c) An integrated capacitor
d) A minimal probing structure

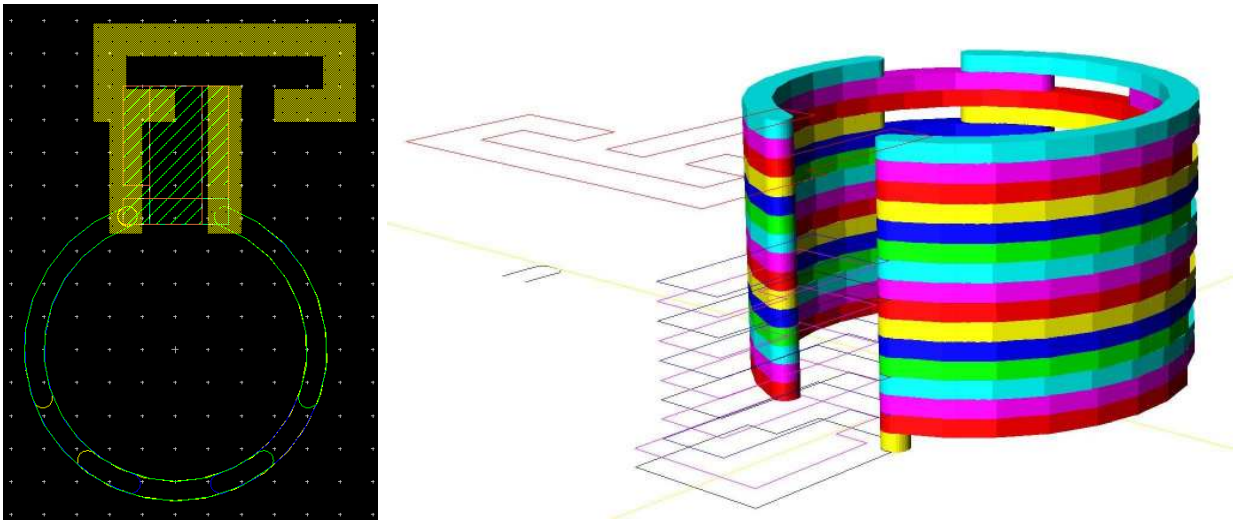


FIGURE 7.1: DEEP-LOOP RESONATOR

The results in Figure 7.2 are encouraging. Qs of almost 80 were measured with the basic s11 method. As stated previously, an error as small as 1% in Γ could mean the actual value is near the estimated value (See Figure 4.3). Also, the structure was designed to resonate at 500MHz. It is actually doing so at 2GHz. This indicates that some of the plates forming the parallel cap may not be connected to the inductor. This seems especially reasonable when the very small area of overlap between the ends of the loop and plates is considered.

This structure was designed to examine the potential for resonators in FTTF. As stated in the **Analysis** section, having a 'tall' conductor with respect to the axis of the solenoid is crucial to obtaining high Qs. For this reason, the one-turn inductor forming the loop might be the best example of the potential of FTTF inductors. No pads were added for external capacitors because of the desire to have a probing structure that would interfere the least with the operation of the resonator. It is unfortunate that more flexibility was not built into the structure, and/or that there are no example of just the loop portion of the resonator. The results may have been very interesting.

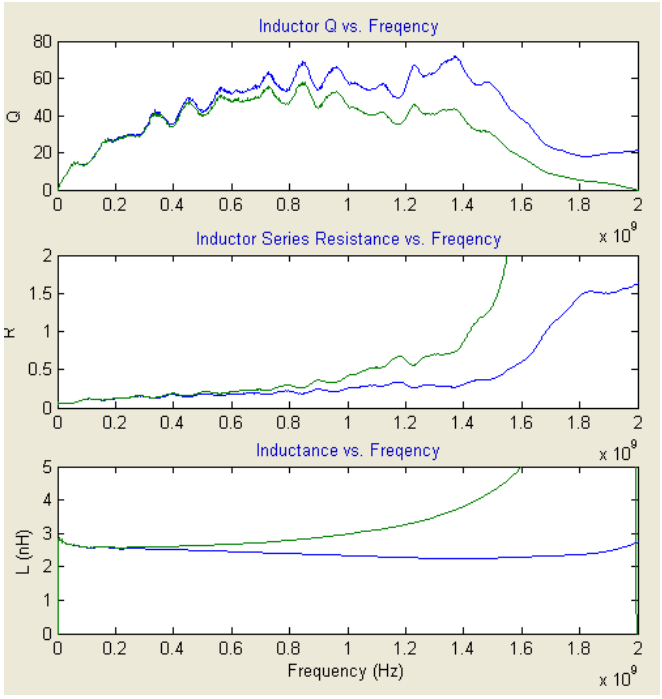


FIGURE 7.2: MEASURED RESULTS OF THE DEEP-LOOP RESONATOR

7.2 2-POLE FILTER

One application that would benefit greatly from high-Q inductors would be filters. Currently, RFICs needing high Q analog filtering must rely on costly off chip components which introduce significant parasitics. FTTF LTCC offers the freedom to create complex 3-dimensional structures directly below the IC. To this end we have developed the two-pole filter prototype shown in Figures 7.3-7.5.

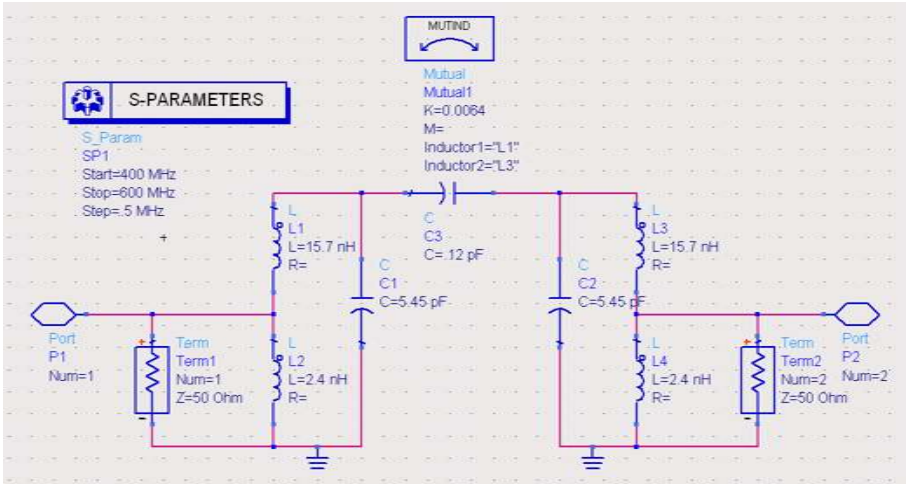


FIGURE 7.3: CONFIGURATION OF THE PROPOSED 2-POLE FILTER

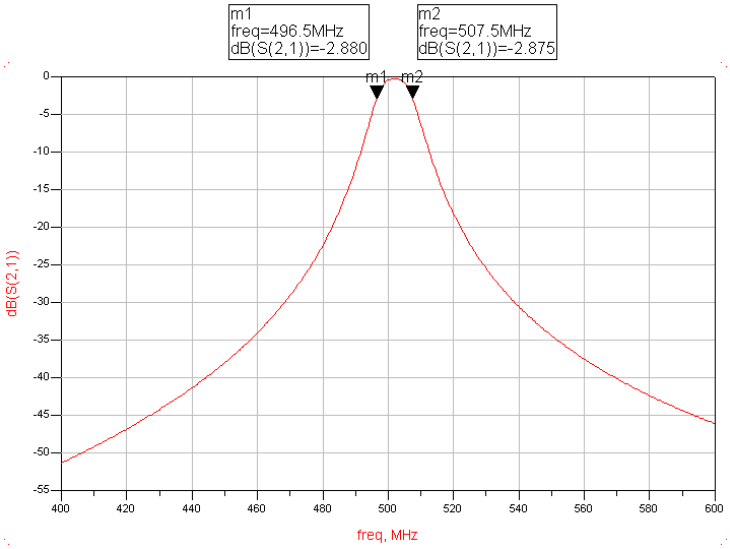
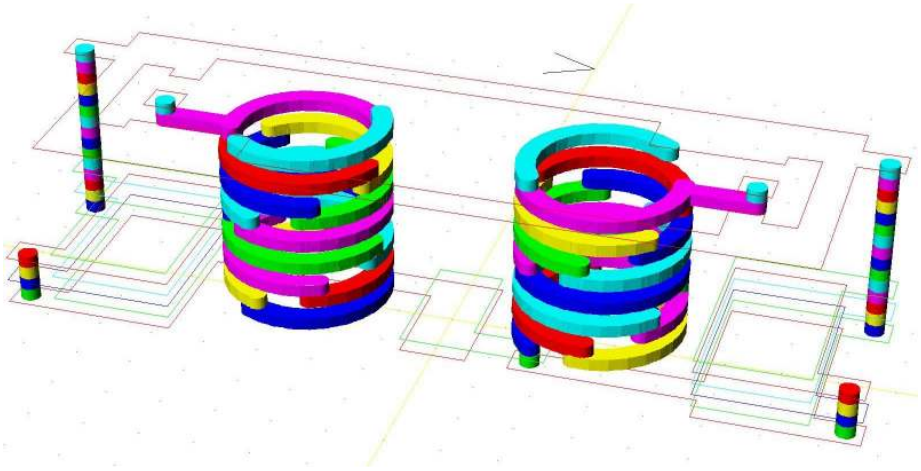
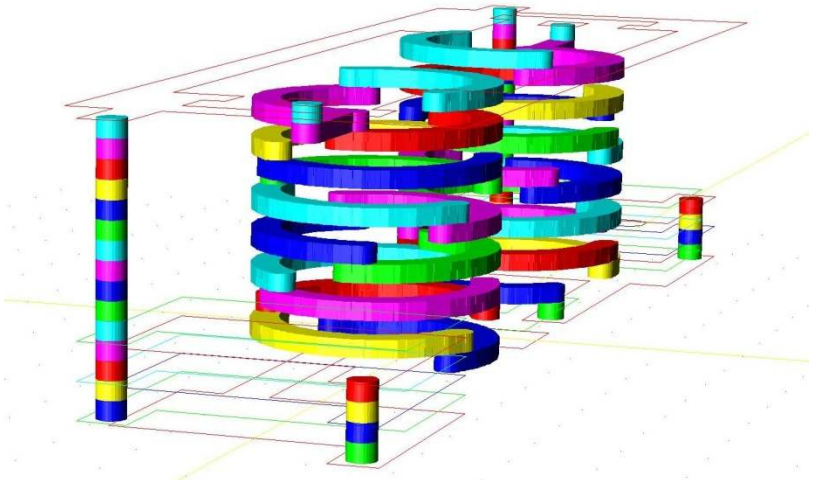


FIGURE 7.4: SIMULATION OF THE FILTER



a



b

FIGURE 7.5: A FTTF 2-POLE FILTER. ALL 2-D FLAT METAL TRACES AND CAPACITORS ARE SHOWN AS OUTLINES.

To match the input impedance of the VNA, the input and output are taps .8 turns from the grounded end of each coil. The flat metal features in the layout are again represented by outlines. They form the parallel caps and the center coupling cap. Each cap has one of its plates on the bottom most layer and was designed to be somewhat larger than the design calls for. The filter can be tuned by manually trimming metal off of these exposed plates. Trimming the parallel caps raises the center frequency and trimming the coupling cap reduces the coupling coefficient.

The fabricated filter shows significant promise but some issues (See Figure 7.6). The design was intended to be centered at 500MHz. The manufactured product operated at ~600MHz. Because the center frequency was already too high, trimming the parallel caps could only raise this further. There also appears to be more coupling capacitance between the coils than was expected. In Figure 7.6l, the coupling cap has been completely removed. This is not surprising given that very small changes in this value can have large impacts on the shape of the filter response. The main problem, however, appears to be that the two poles are not centered at the same frequency. This could be caused by a fabrication problem in the caps. Even with these flaws, this structure demonstrates the feasibility of integrated multi-pole filters. A modified design could possibly be fabricated to interface directly with on-chip circuitry.

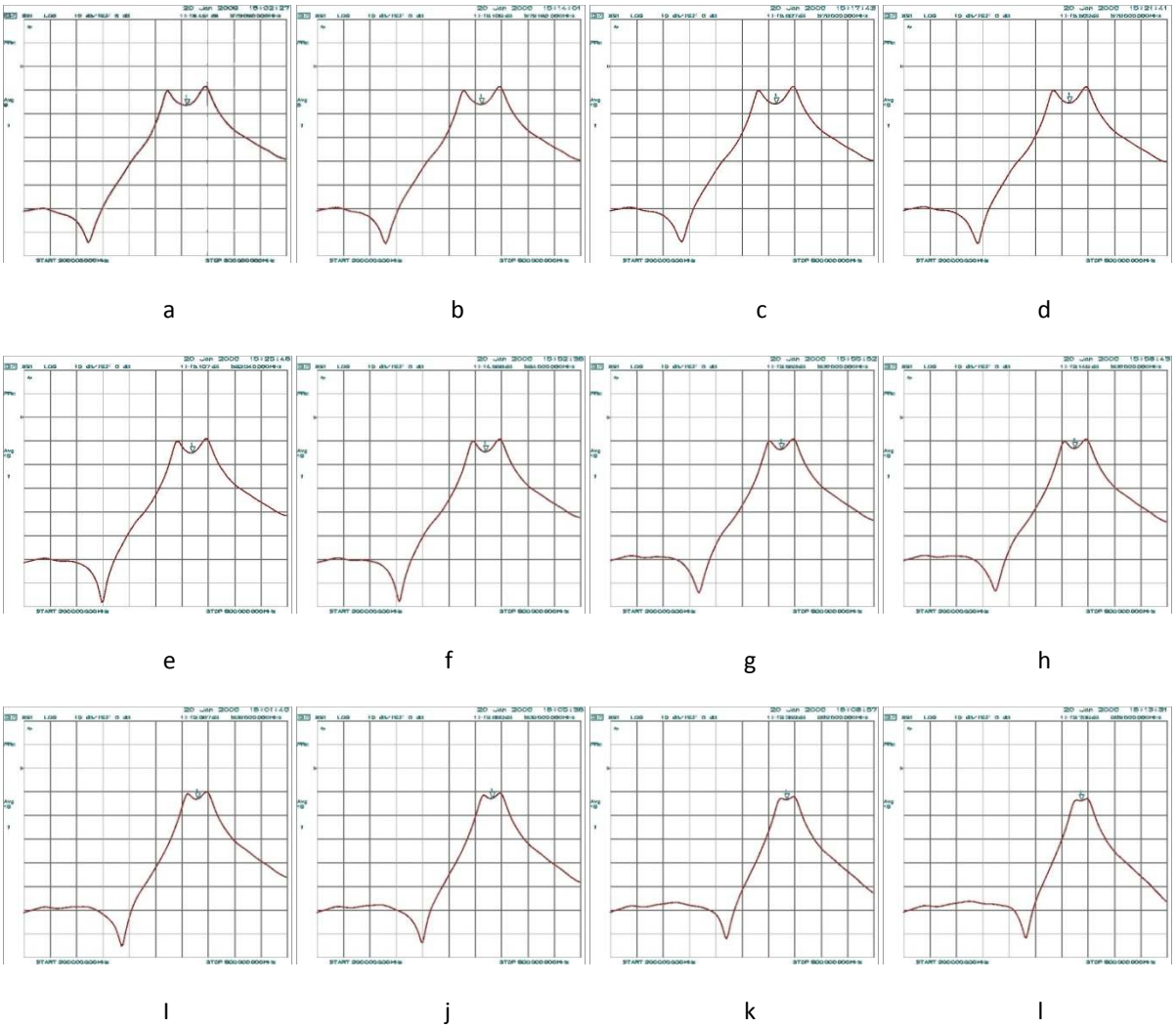


FIGURE 7.6: PROGRESSION OF 2-POLE FILTER RESPONSE AS COUPLING CAP IS TRIMMED

SECTION VIII - CONCLUSION

By applying a novel technique, FTTF, we have prototyped an array of high-Q inductors in LTCC. This was done to evaluate their performance, explore their design requirements, and lay the groundwork for future development of FTTF inductors. Estimations of L, Q, and SRF were made for some of the simpler inductors. The array was fabricated and measured using multiple techniques to validate the results. The results, while not meeting our preliminary optimistic projections, do lead to some interesting and useful conclusions.

Most important of these is the promise this work shows. Even as they are, most of these inductors demonstrate higher Qs than what is available for any integrated inductor. For example, Qs of 60 have been proven to be viable at 500MHz for the larger 80mil diameter designs. This is consistent with values achieved at this frequency by commercially available surface mount devices. With further development, it is likely that even higher Qs can be achieved.

By themselves, these inductors could be useful in any number of applications where the parasitics associated with going off-chip and then back again are acceptable. These can be limited to bondwire or solder bump parasitics if the component is located directly below the IC. Another potential application is in compact power systems, such as switching regulators. These operate in the 1-10MHz range. At these frequencies SRF can be very low, and so very high-Q structures can be designed with less stringent restrictions on internal capacitance. In the end, their real strength may be in the development of passive multi-pole filters which would be impractical to implement in silicon and too fragile for many high-reliability applications. A filter could be made to be even more useful if it were combined with active on-chip circuitry or post-manufacture trimming that could ensure that the poles are properly aligned with their intended center frequency.

8.1 FUTURE WORK

There are several facets of this work which have presented themselves as question marks or outright problems to be avoided or studied in future work.

- The probing structure we used was intended to be a flexible as possible. There is a possibility that it hinders the measurements just by being present. Pads for the series cap are necessary for the s21 measurement, but the pads for the two parallel caps could be omitted.
- 'Empty' probing structures, which have a short instead of an inductor, were included in the array. The hope was that these could be measured and used to remove the effects of the probing structure from the inductors in a post-process. This was not done so it is unknown how helpful it would have been.
- The shape of the s11 curve was observed to significantly degrade when the second probe was moved over inductors. This indicates that the s21 measurement, which must have the second probe present, could also be giving questionable results. A better arrangement for the probing structure would be one where neither probe passed over the center of the inductor.
- To help maximize Q, maximize the conductor surfaces which are parallel to the axis of the solenoid.
- Do not use a punch with a diameter smaller than the thickness of the tape being punched.
- The horizontal inductors (**G**s and **H**s) had an especially low yield. This indicates that they are more susceptible to fabrication problems. However, this may not be a problem if larger punch sizes are used.
- If a ground shield is called for, use a picket fence-style of shield made out of individual vias instead of the nearly solid wall used in these designs.

- When electrically connecting any two features (flat or FTTF) on different layers, design for an overlap area which is large enough to ensure connection even if the features are off by more than the tolerance of the fabrication process.
- Try to avoid placing FTTFs in the top-most or bottom-most layers of ceramic. It is possible for the metal paste in these to crumble and fall out.
- The lower conductivity of the gold paste used is only half that of normal gold. A higher-conductivity paste such as silver should be considered.
- The exact conductivity of the gold paste is not known. The value we used (2.22s/m) was calculated from the dc resistance of the one-layer spiral, **K3**, found using a four-wire resistance measurement. To establish conductivity, future trials should have a set of structures specifically designed for this measurement made of both flat features and FTTFs.
- There may be benefit into studying the performance of FTTF spiral inductors, like those presented in [15]. The spirals in this work are all made with flat metal.
- The deep loop resonator was one of the only structures in the array without pads for resonating caps. It should have been above and beyond the highest-Q structure. We would have been able to answer several questions and confirm some conclusions if it were possible to look that the s21 measurement of that structure.
- In these measurements, no factory-specified calibration coefficients for the probes were entered into the VNA. A full 2-port calibration was performed, but using these coefficients would eliminate one more possible source of errors.

It is our hope that the information provided here will be useful for anyone interested in developing FTTF LTCC passive components. This work has identified many of the obstacles that need to be overcome before judgment can accurately be passed on the ultimate performance possible with the FTTF technique.

"Piled Higher and Deeper" by Jorge Cham

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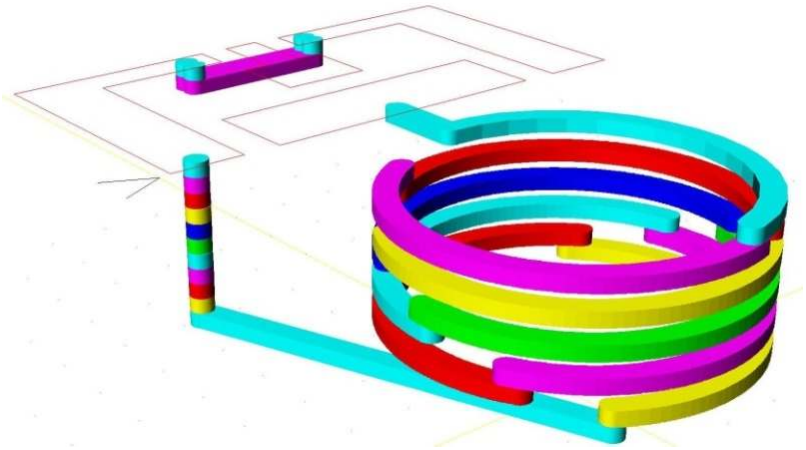
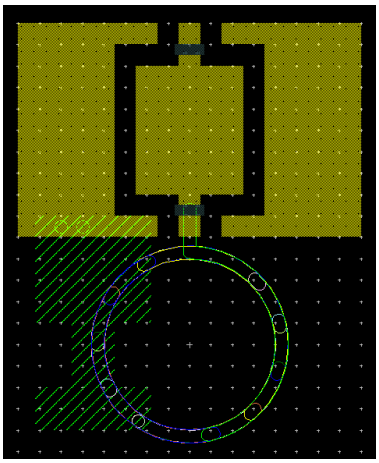
APPENDIX

This appendix contains descriptions and images of the various types of inductors included in the array, as well as initial estimations for selected structures. Also provided are Q plots taken from s11 measurements. In these, there are two lines. The green line represents the raw data recorded from the VNA. The blue line represents the performance of the pure ideal inductor. This is calculated by mathematically subtracting the internal capacitance (or more specifically, the admittance of the internal capacitance) from the raw plot. This can be thought of as a 'truer' measure of L and Q because, while the internal capacitance will be there in any application, a good design will account for its presence. Therefore, it is helpful to see the ideal inductance without those effects present.

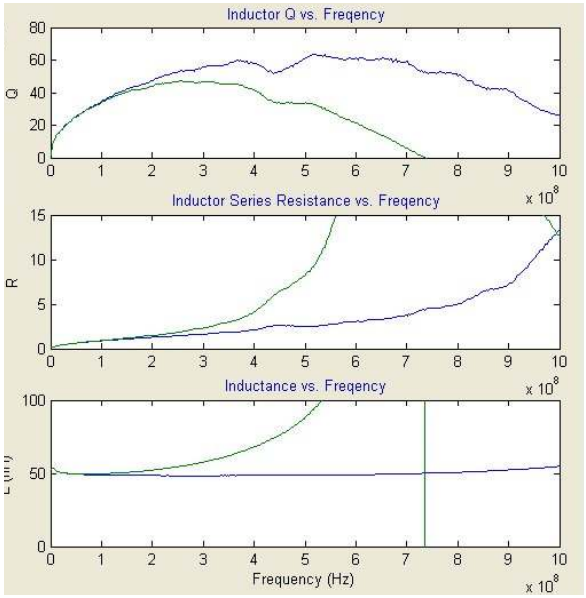
A: Solenoid

This variety is the most straightforward implementation of the FTTF concept to solenoid inductors. Each half-turn is cut into a tape layer. The turn is continued in an adjacent layer. There is only one layer of tape separating the turns. Using thinner tapes will result in a lower SRF and Q. Increasing the punch diameter will decrease the SRF but will not help the Q at higher frequencies.



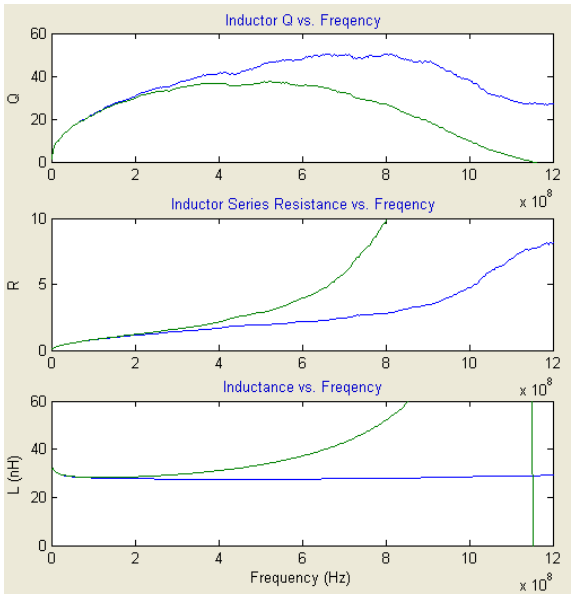


A1: 80mil dia, 7mil punch, 10 layers



Est. L = 52nH, Est. Q(500MHz) = 59, Est. SRF = 1.5GHz

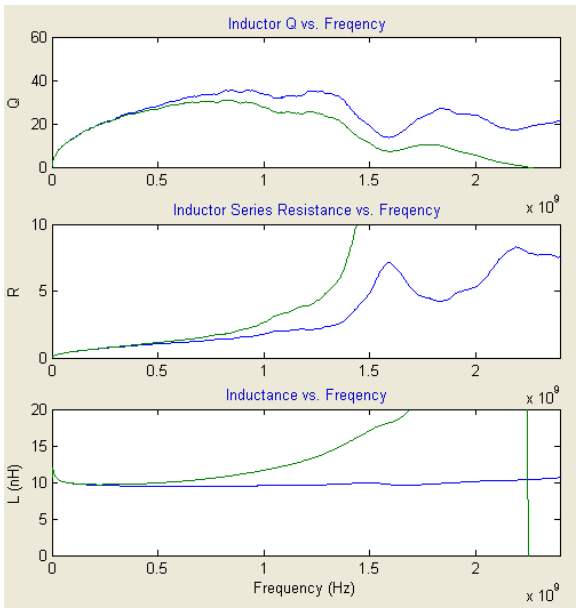
A4: 40mil dia, 7mil punch, 15 layers



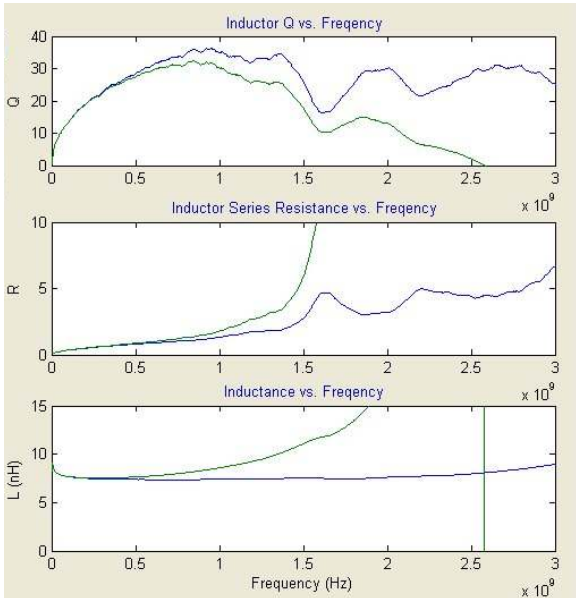
Est. L = 29nH, Est. Q(500MHz) = 47, Est. SRF = 3.4GHz

A5: 20mil dia, 7mil punch, 15 layers

A6: 20mil dia, 7mil punch, 10 layers

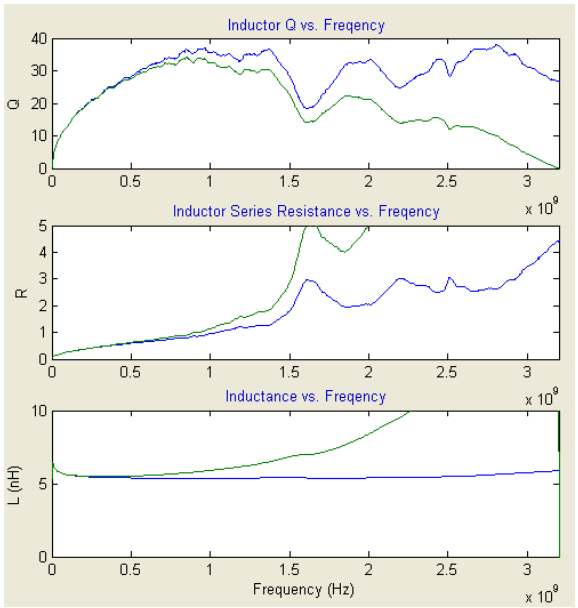


Est. L = 8.4nH, Est. Q(500Mhz) = 30, Est. SRF = 8.0GHz



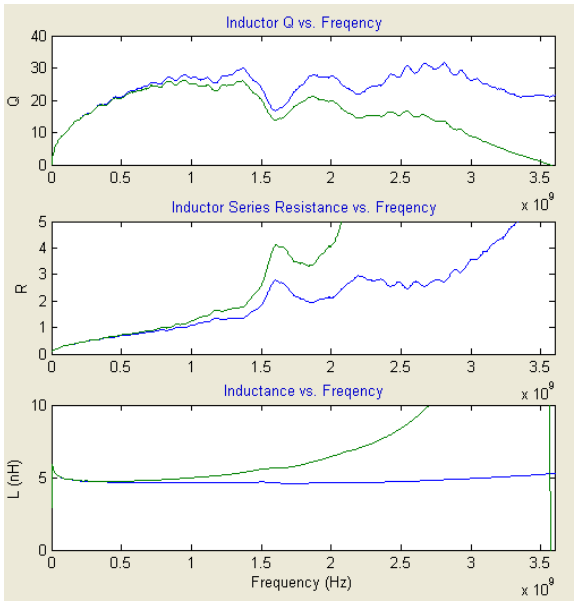
Est. L = 5.2nH, Est. Q = 27, Est. SRF = 7.9GHz

A7: 20MIL DIA, 7MIL PUNCH, 5 LAYERS



Est. L = 2.1nH, Est. Q(500Mhz) = 23, Est. SRF=7.1GHz

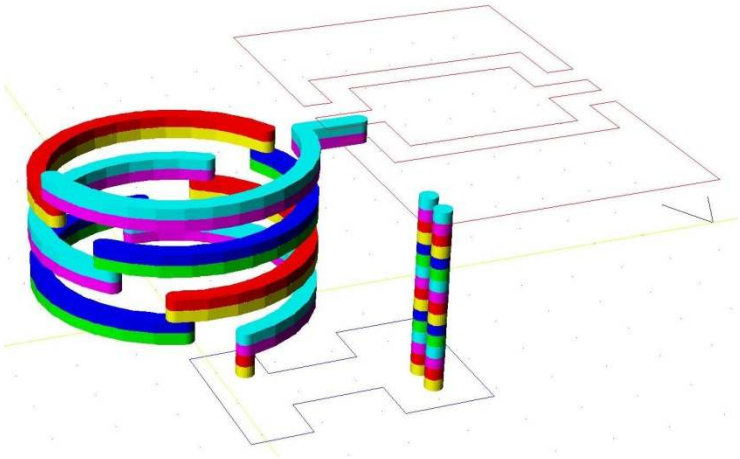
A8: 10MIL DIA, 7MIL PUNCH, 5 LAYERS

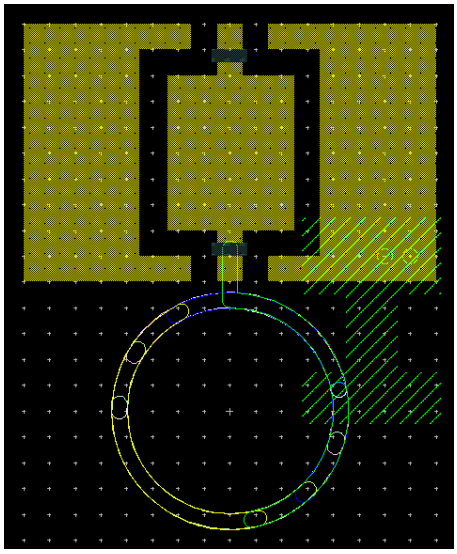


Est. L = 0.6nH, Est. Q(500Mhz) = 16, Est. SRF = 13GHz

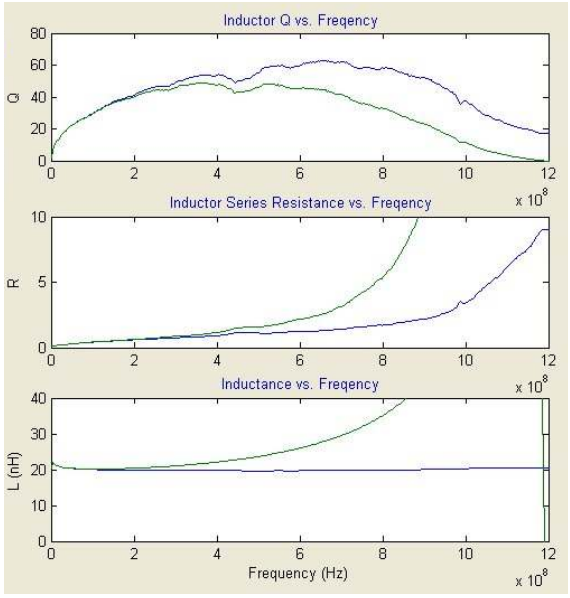
B: Double-Thickness Solenoid

By doubling the thickness of the tape used, the turns become thicker and separated by larger gap. This helps raise SRF and Q. Because of fabrication limitations, a thicker tape was simulated by stacking pairs of identical layers. However, this means that for a given substrate the overall number of turns possible is cut in half.



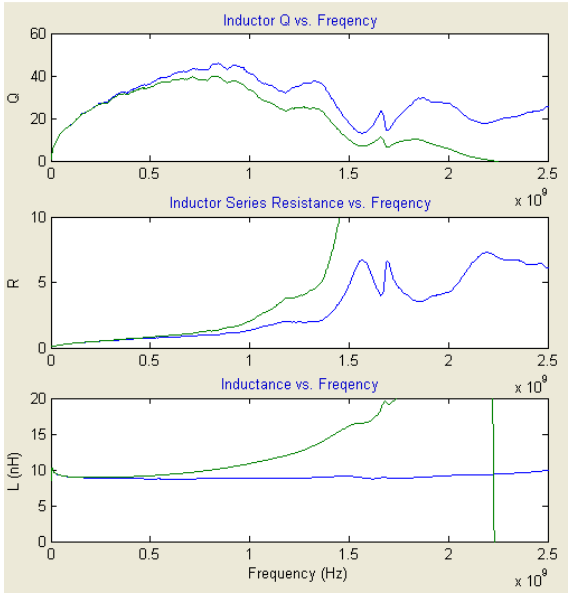


B1: 80mil dia, 7mil punch, 7 layers



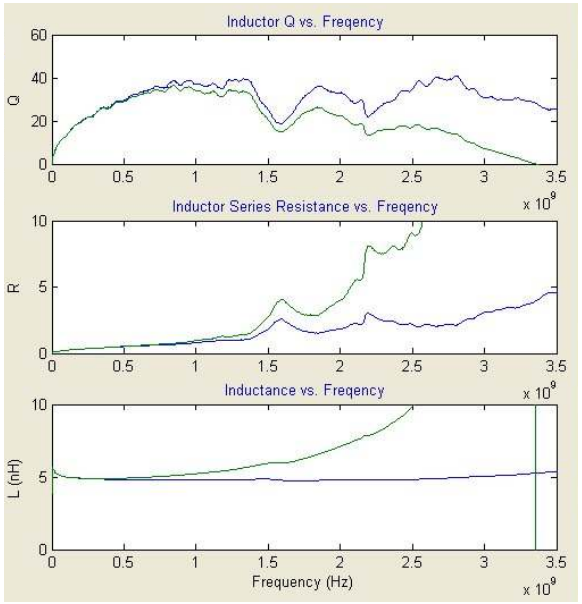
Est. L = 21nH, Est. Q(500Mhz) = 69, Est. SRF= 2.7GHz

B4: 40mil dia, 7mil punch, 7 layers



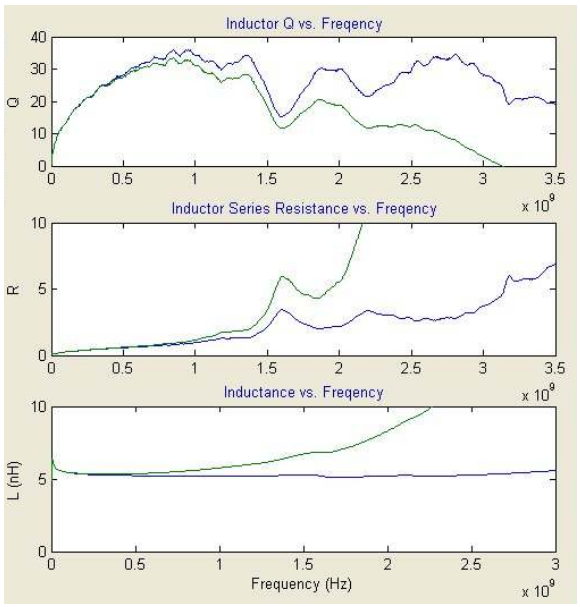
Est. L = 6.7nH, Est. Q(500Mhz) = 46, Est. SRF= 6.2GHz

B5: 40MIL DIA, 7MIL PUNCH, 3 LAYERS



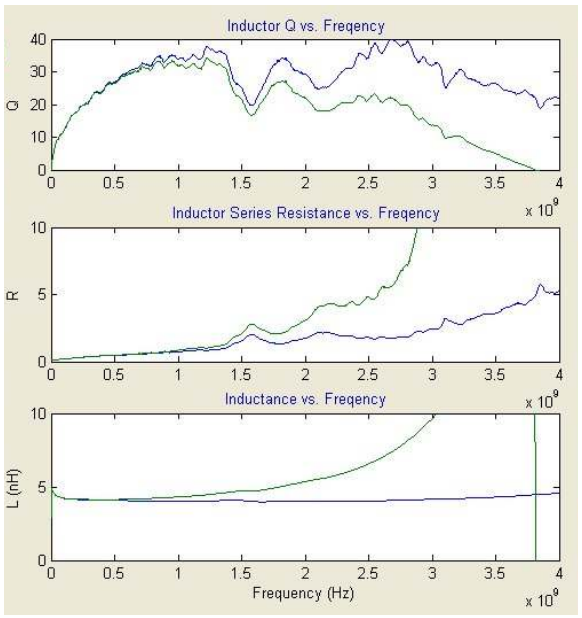
Est. L = 2.1nH, Est. Q(500Mhz) = 33, Est. SRF = 4.3GHz

B6: 20MIL DIA, 7MIL PUNCH, 7 LAYERS



Est. L = 1.9nH, Est. Q(500Mhz) = 30, Est. SRF = 14GHz

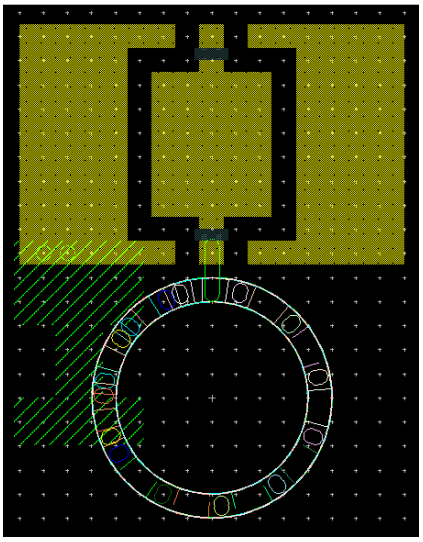
B7: 20 MIL DIA, 7MIL PUNCH, 3 LAYERS

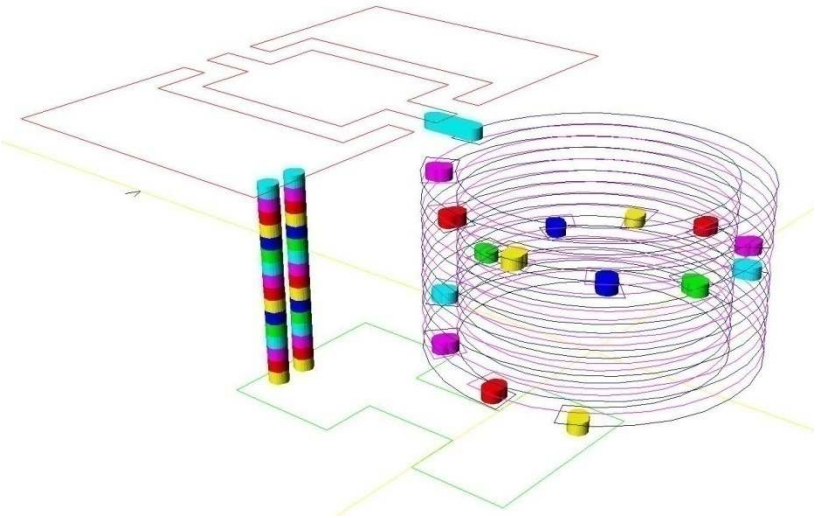


Est. L = 6.7nH, Est. Q(500MHz) = 24, Est. SRF = 7.2GHz

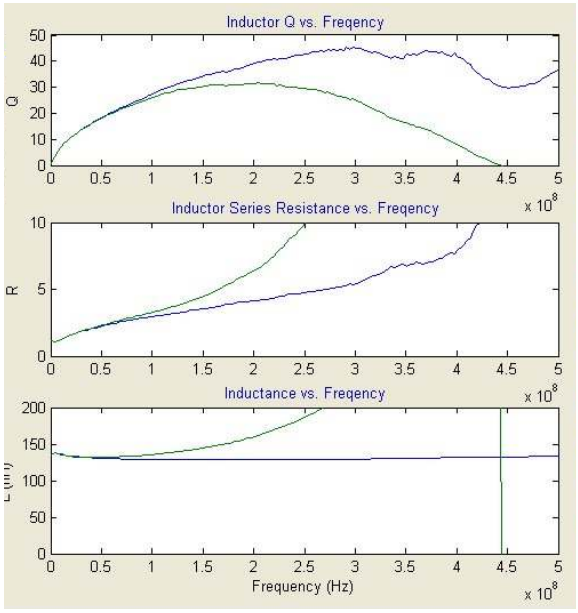
C: Flat Metal Solenoid

This variety applies the idea of solenoidal inductors to the traditional LTCC technique of printing a thin layer of metal which is sandwiched between layers of tape. The vias here are only utilized as traditional vias, to connect two layers. Because the 'adjacent layer' design constraint does not apply here, a full turn can be placed on each layer.



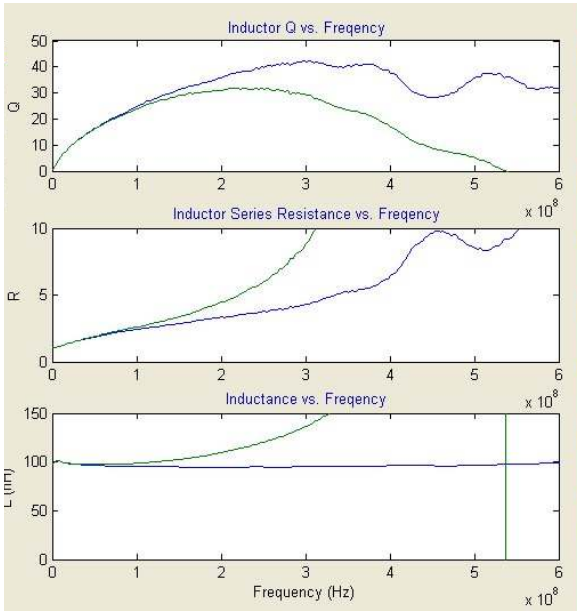


C1: 80mil dia, 8 Turns, 1 layer spacing, 10mil wide



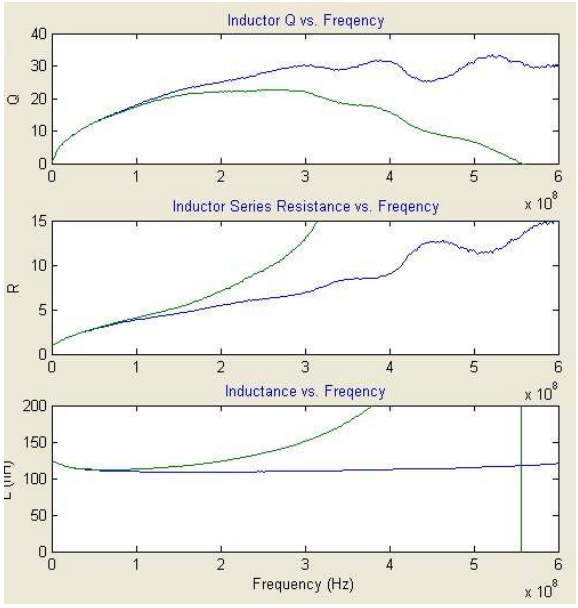
Est. L = 164nH, Est. Q(500MHz)= 17, Est. SRF= 1.1GHz

C2: 80mil dia, 8 Turns, 2 layer spacing, 10mil wide



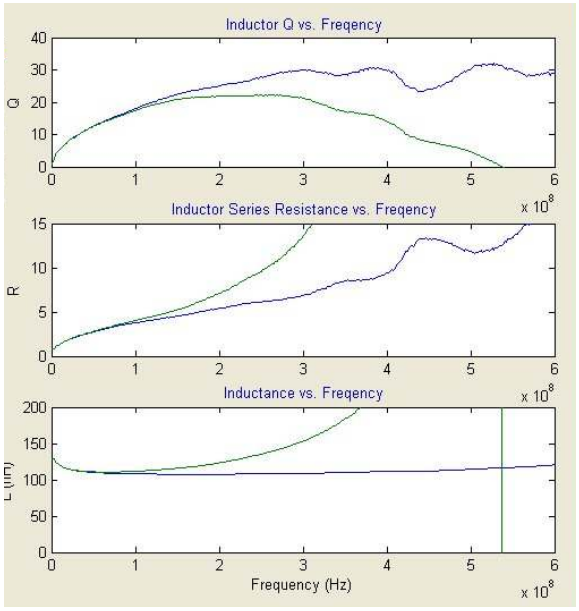
Est. L = 110nH, Est. Q(500MHz)= 11, Est. SRF= 1.6GHz

C3: 40MIL DIA, 15 TURNS, 1 LAYER SPACING, 10MIL WIDE



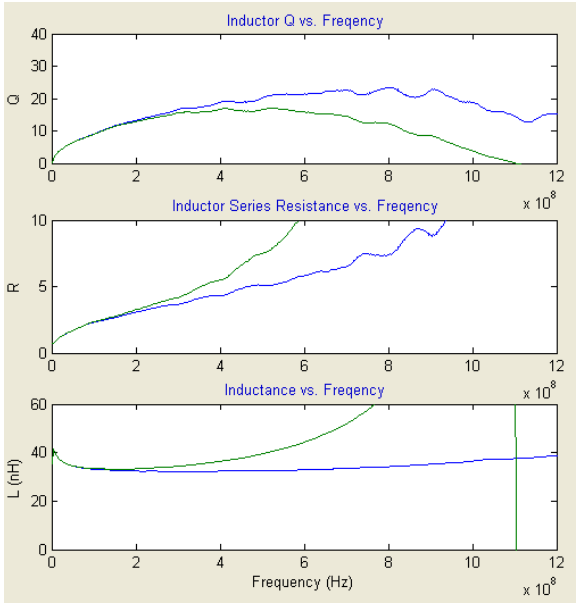
Est. L = 120nH, Est. Q(500MHz)= 13, Est. SRF= 2.0GHz

C4: 40MIL DIA, 15 TURNS, 1 LAYER SPACING, 15MIL WIDE



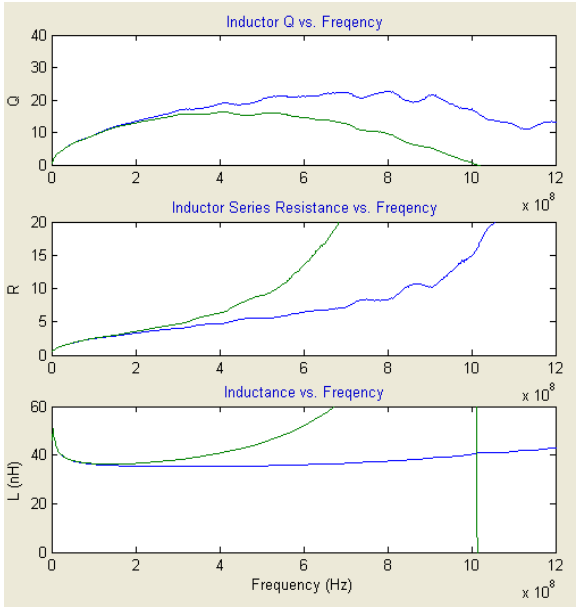
Est. L = 120nH, Est. Q(500MHz)= 13, Est. SRF= 1.6GHz

C6: 20MIL DIA, 15 TURNS, 1 LAYER SPACING, 10MIL WIDE



Est. L = 34nH, Est. Q(500MHz) = 7.4, Est. SRF= 4.9GHz

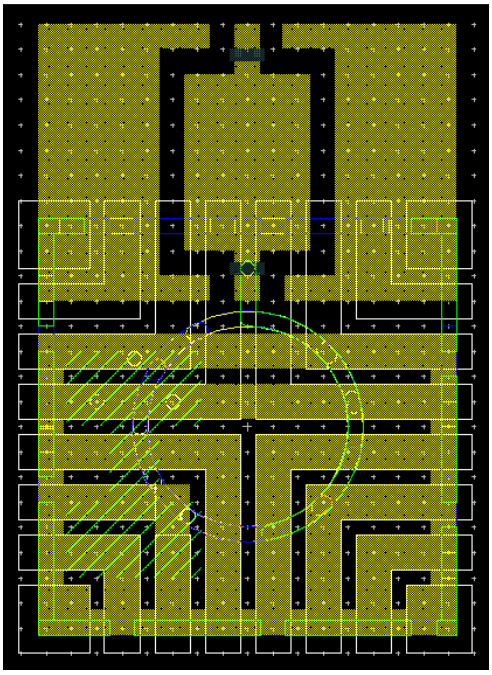
C7: 20MIL DIA, 15 TURNS, 1 LAYER SPACING, 15MIL WIDE

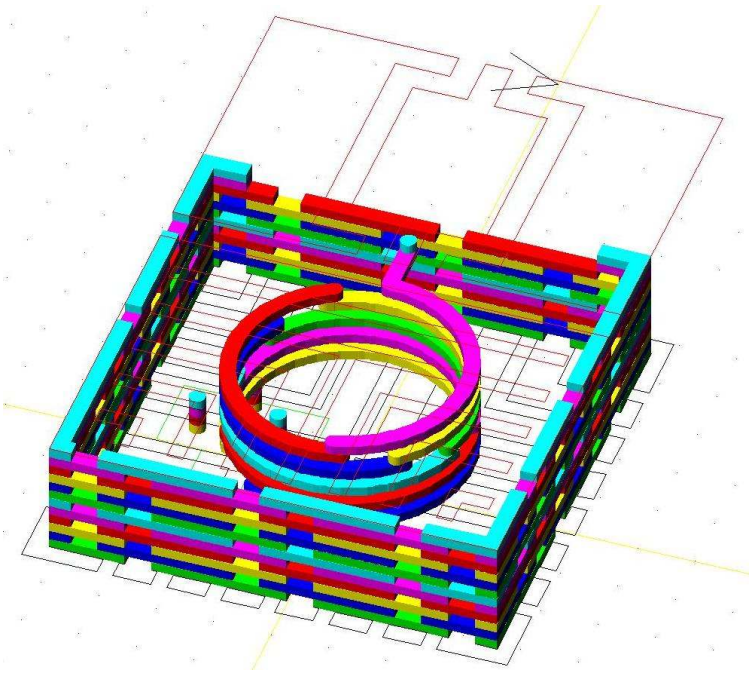


Est. L = 34nH, Est. Q(500MHz) = 7.4, Est. SRF= 3.7GHz

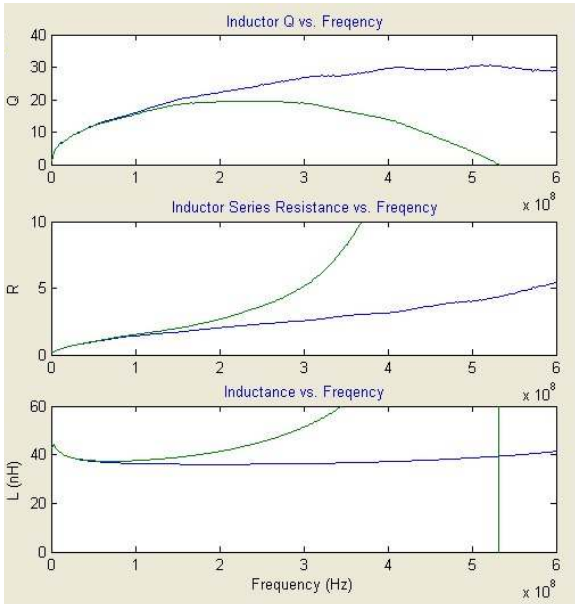
D: Solenoid with Cage

In a real-world application, it may be helpful to shield the inductor from outside influences and vice-versa. Variety 'D' is similar to variety 'A'. However, there is a nearly solid wall of vias surrounding it forming a ground shield. This wall, or fence as we call it, has multiple opening in differing places on any given layer. This is to provide structural support for the tape making up the area between the fence and inductor. There are also variations allowing for the top and bottom planes to be solid metal, patterned metal, or open. All inductors are 10 layers.

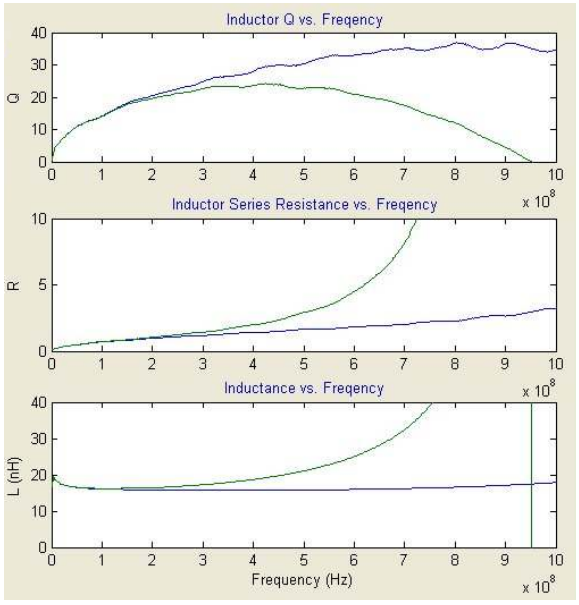




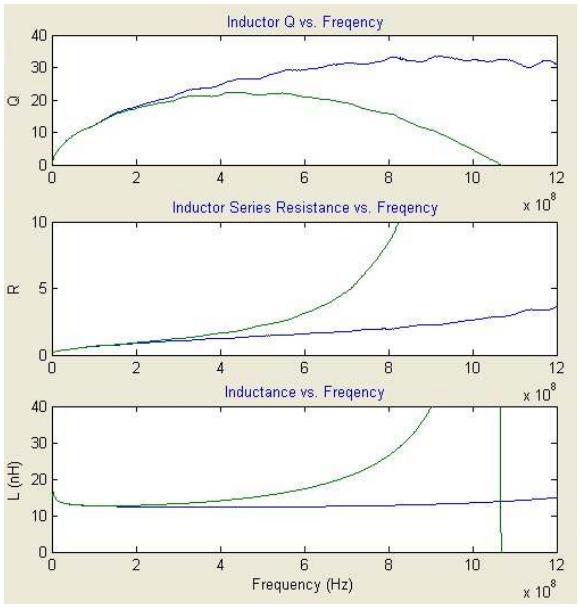
D1: 80mil dia, patterned, 7mil punch



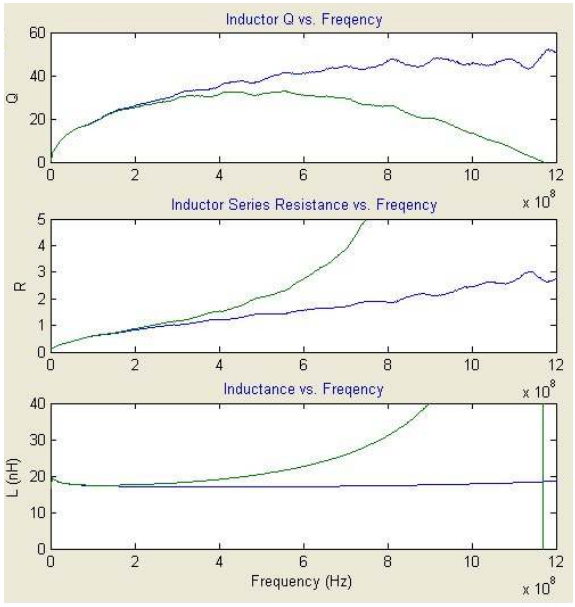
D4: 40mil dia, patterned, 7mil punch



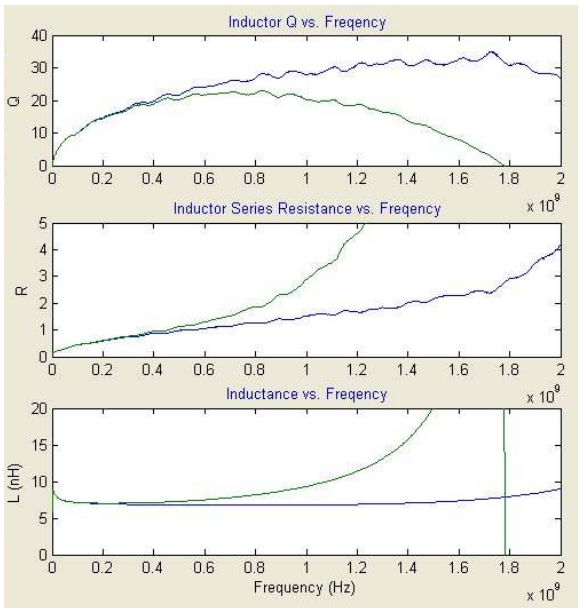
D5: 40MIL DIA, SOLID, 7MIL PUNCH



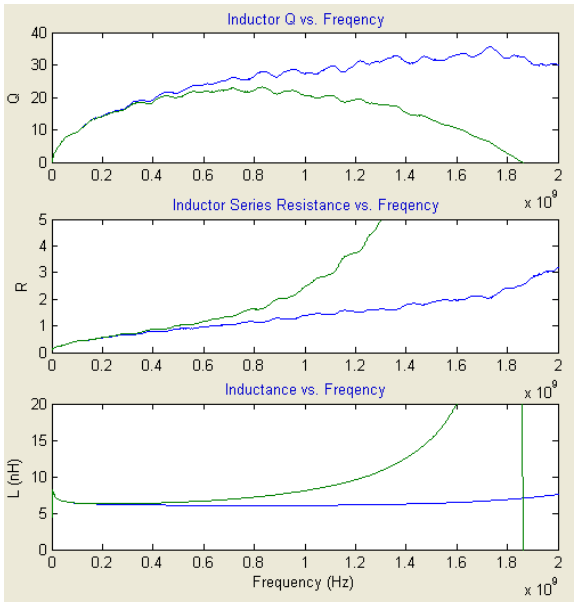
D6: 40MIL DIA, OPEN, 7MIL PUNCH



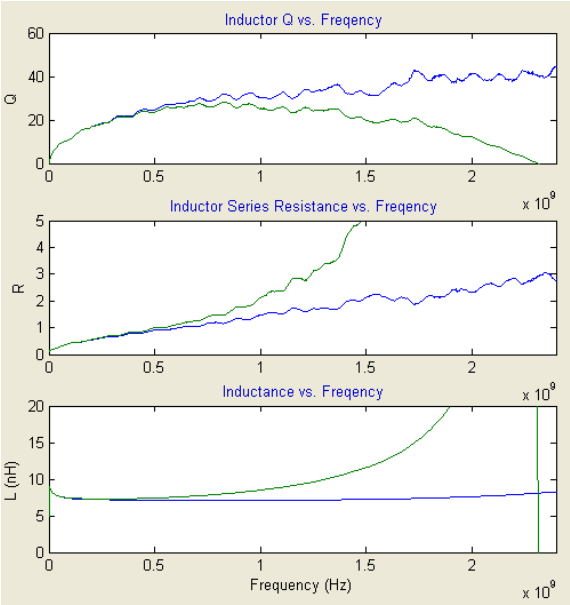
D7: 20MIL DIA, PATTERNED, 7MIL PUNCH



D8: 20MIL DIA, SOLID, 7MIL PUNCH

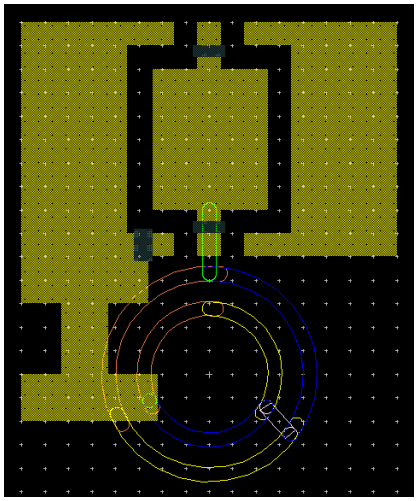


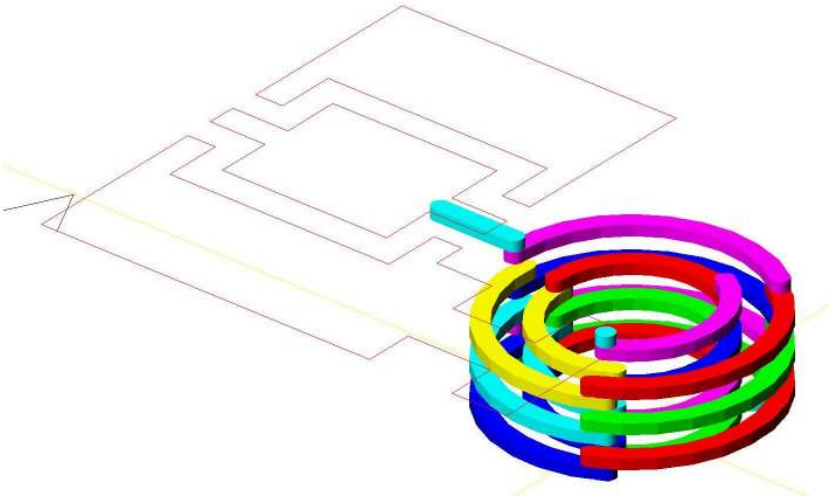
D9: 20MIL DIA, OPEN, 7MIL PUNCH



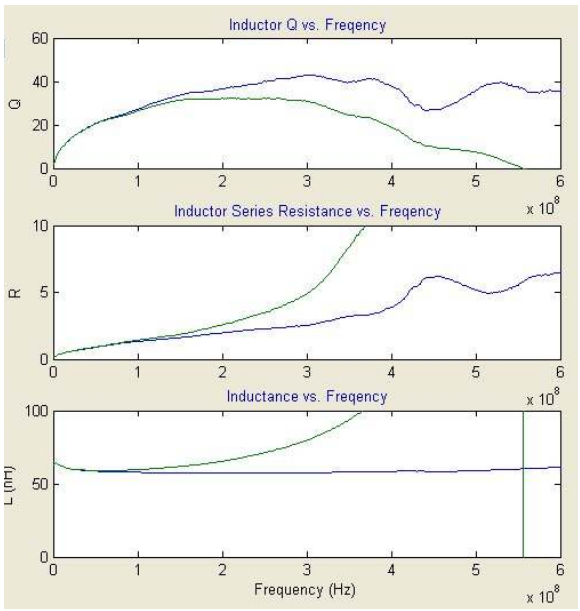
E: Double-Layer Solenoid

This variety was intended to test the possibility of increasing inductance by placing multiple inductor turns on the same layer, like a coil that has multiple layers of turns. The intention was to increase inductance at the cost of lowering the SRF. The design had the added benefit of having the input and output at the top, requiring no via.

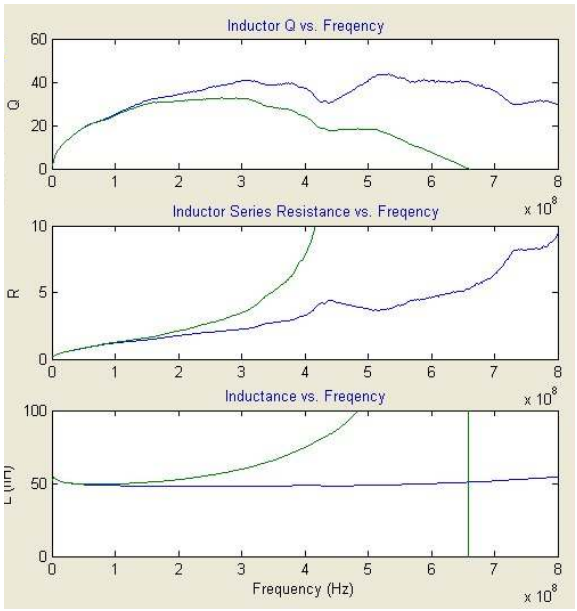




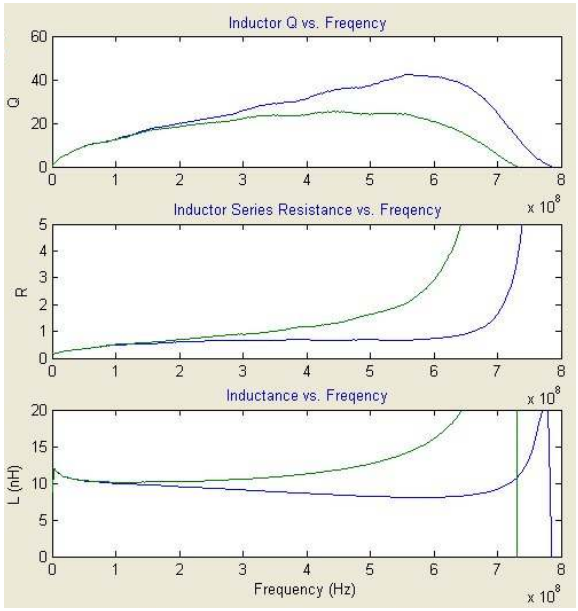
E1: 80mil/50mil dia, 15 layers



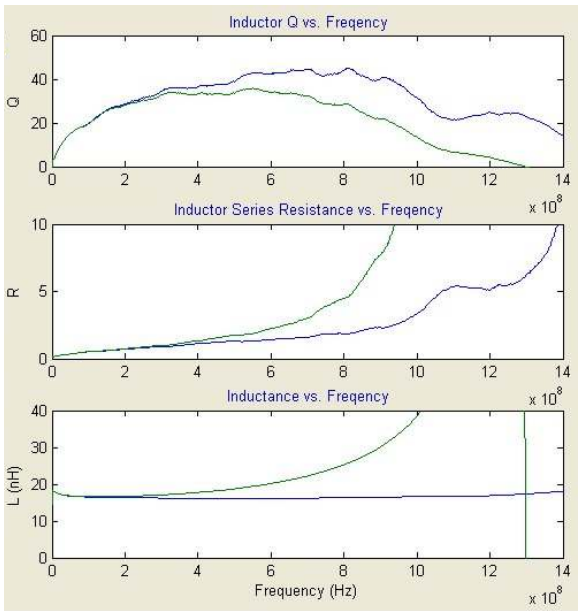
E2: 80mil/40mil dia, 10 layers



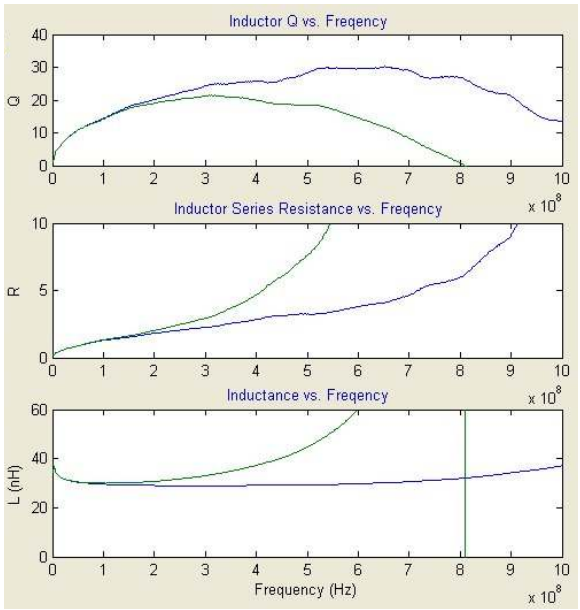
E3: 80MIL/50MIL DIA, 15 LAYERS



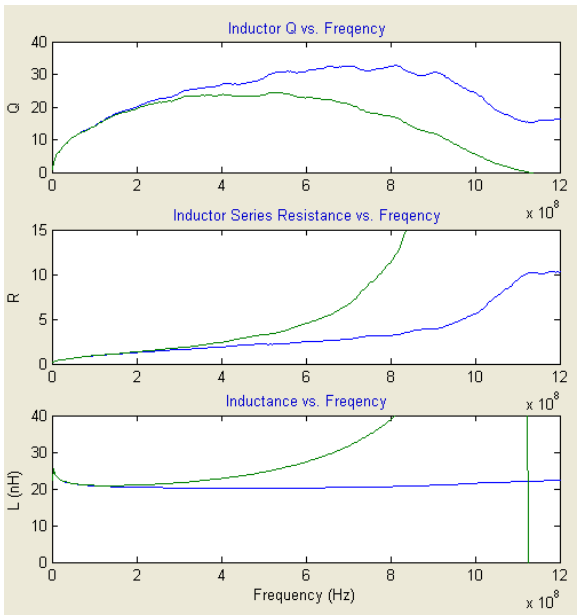
E4: 80MIL/50MIL DIA, 5 LAYERS



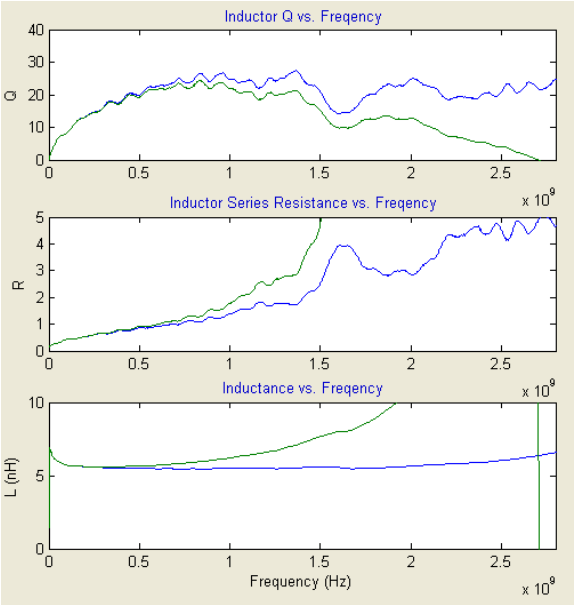
E5: 50MIL/20MIL DIA, 15 LAYERS



E6: 50MIL/20MIL DIA, 10LAYERS

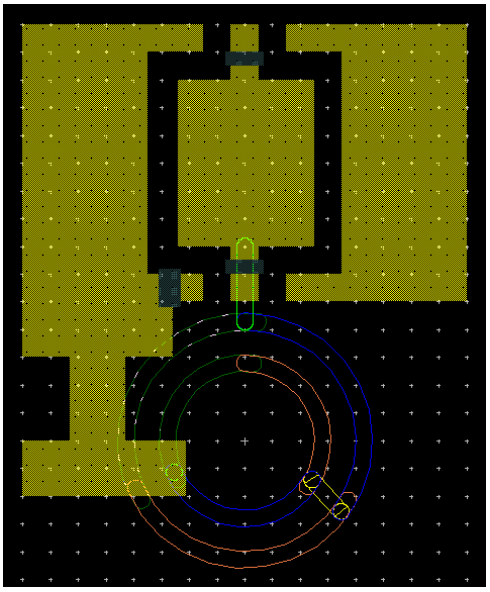


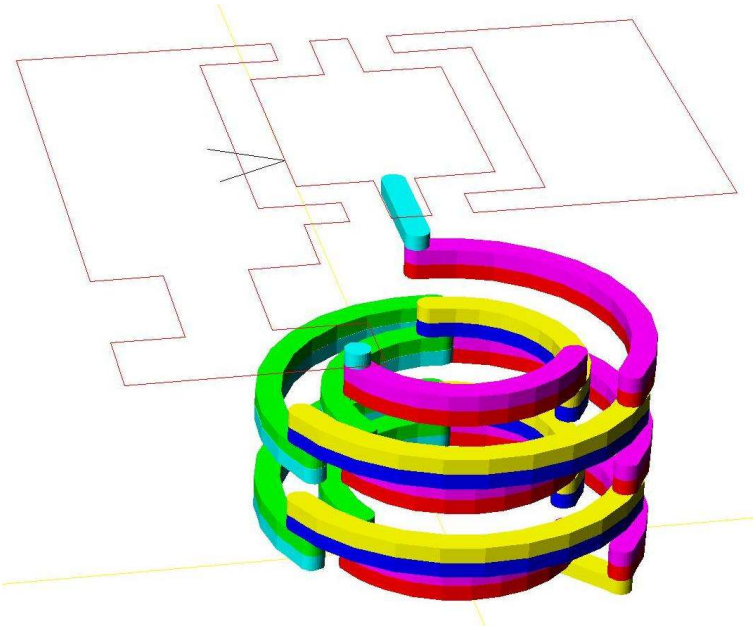
E7: 50MIL/20MIL DIA, 5 LAYERS



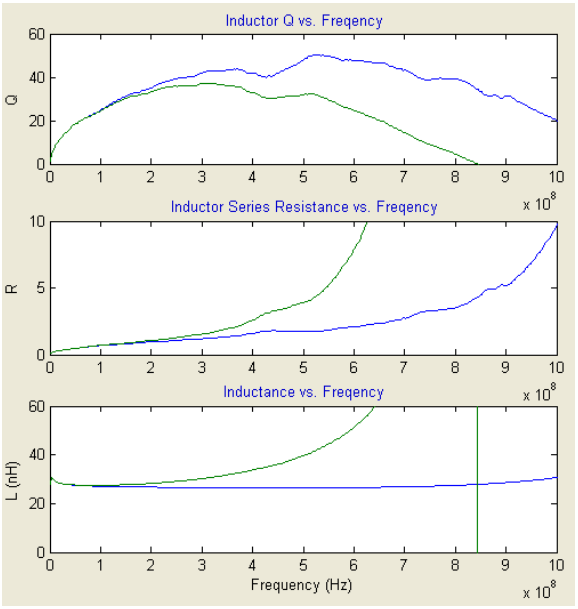
F: Double-Thickness, Double-Layer Solenoid

Variety ‘F’ is very similar to variety ‘E’. The difference is that two identical layers are grouped together to emulate tape which is twice as thick, as in variety ‘B’.

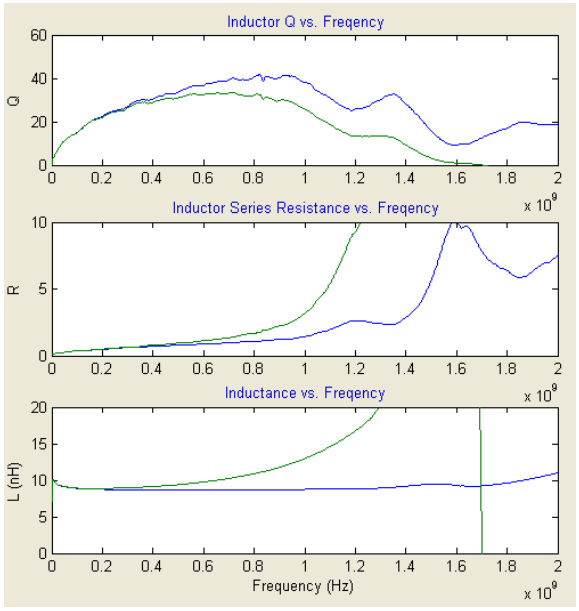




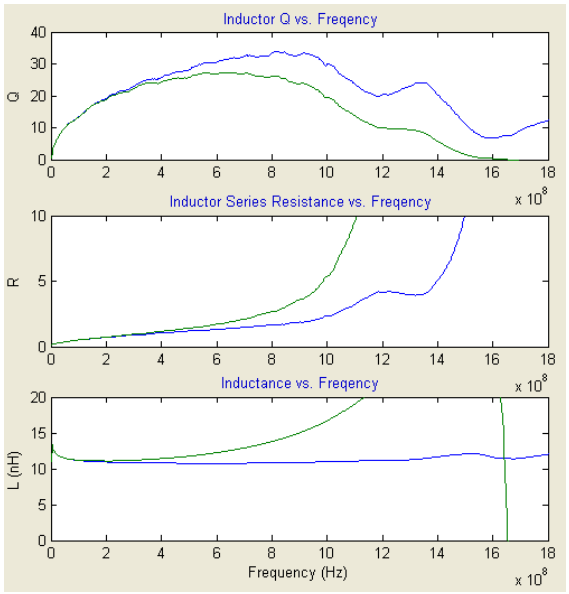
F1: 80mil/50mil dia, 7 layers, 7mil punch



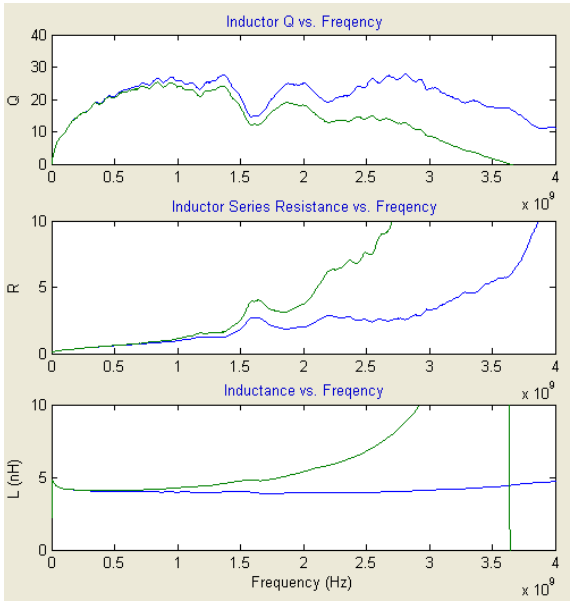
F3: 80mil/50mil dia, 3 layers, 7mil punch



F4: 50MIL/20MIL DIA, 7 LAYERS, 7MIL PUNCH

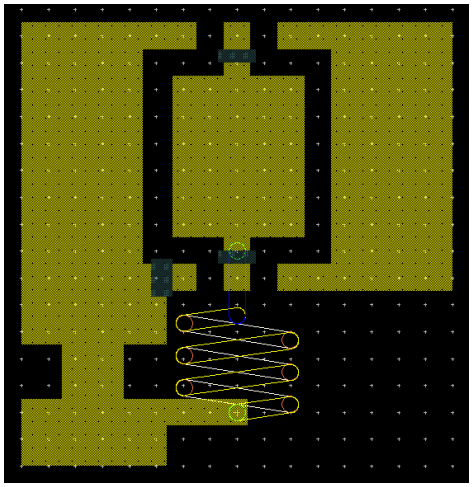


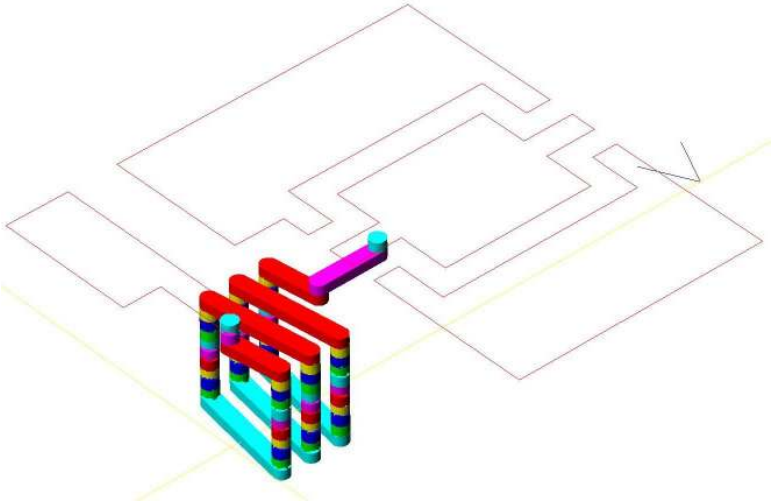
F5: 50MIL/20MIL DIA, 3 LAYERS, 7MIL PUNCH



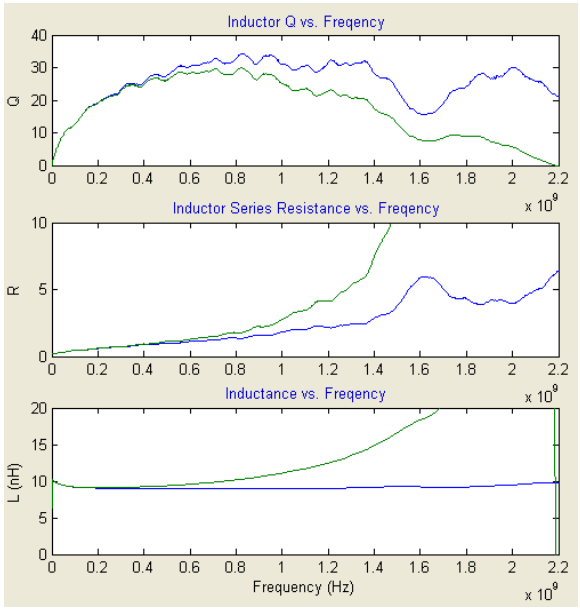
G: Horizontal Solenoid

These inductors differ from the vertical varieties in the orientation of their Z axis, or the dimension along which you consider length. For the vertical varieties, this direction is in parallel with the layers of tape. Straight elements in the top and bottom layers form ½ of each turn. 'Vias' in the traditional sense form the other ½ of each turn. Therefore, each turn passes through each of the interior layers twice. For this reason it becomes simple to discuss them in terms of 'Turns' rather than 'Layers', as in other varieties. These inductors should have several advantages and disadvantages over the vertical ones. Most importantly, there is no theoretical constraint on length; inductance can be increased by simply adding another turn. The ends of the structure can also be placed on any layer of the substrate, rather than requiring one be on the top and one be on the bottom. However, they are constrained in diameter; it cannot be greater than the thickness of the substrate. Also, it is possible that they could be more susceptible to fabrication problems. Because there are far more connections between layers, there are more opportunities for errors.

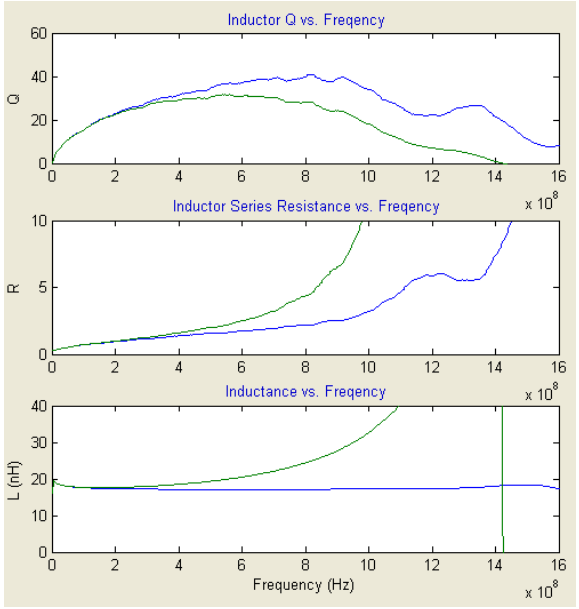




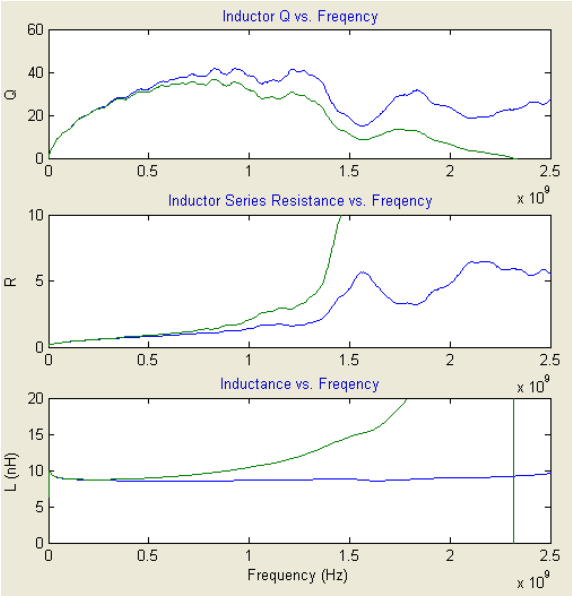
G3: 3 turns, 18mil pitch



G4: 6 turns, 18 mil pitch

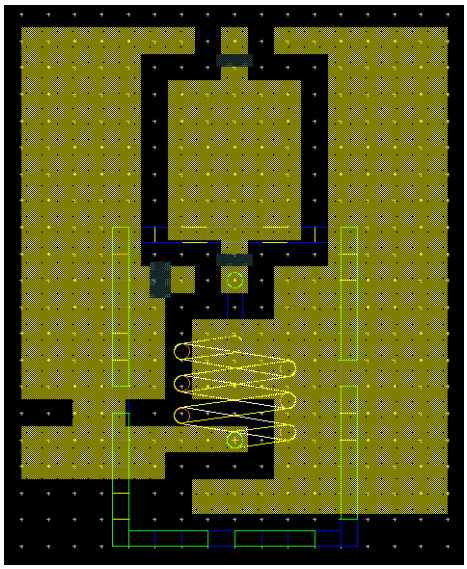


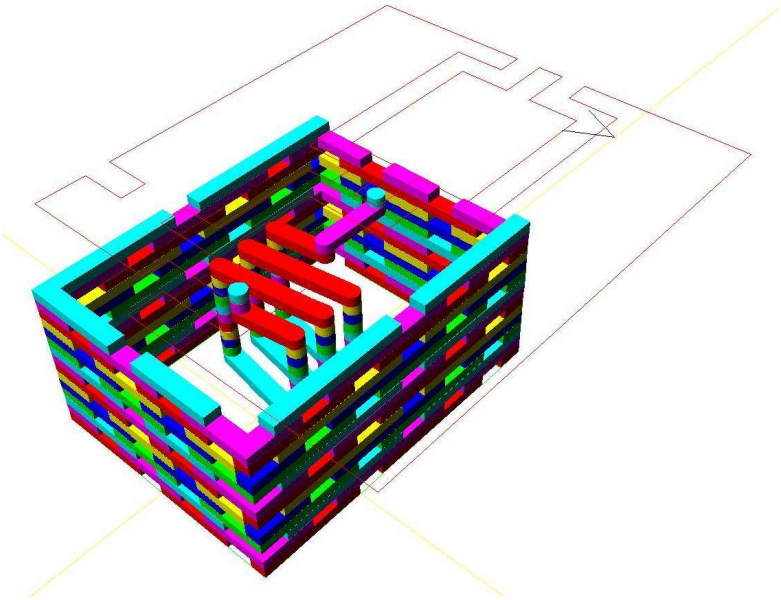
G5: 3 TURNS, 24MIL PITCH



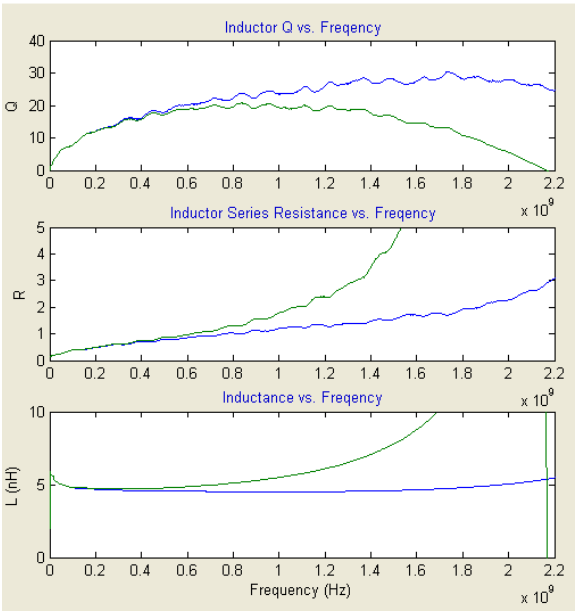
H: Horizontal Solenoid with Cage

This variety applies the idea of using a ground shield to the horizontal inductors. Many of the same issues exist, such as the need for windows in the cage to support the tape on the inside. Because the parts of the shield which cover the ends of the inductor cannot (easily) be formed into a shield, a 'solid' cage is used for all of the structures. The effects of changing the distance between inductor are examined instead.

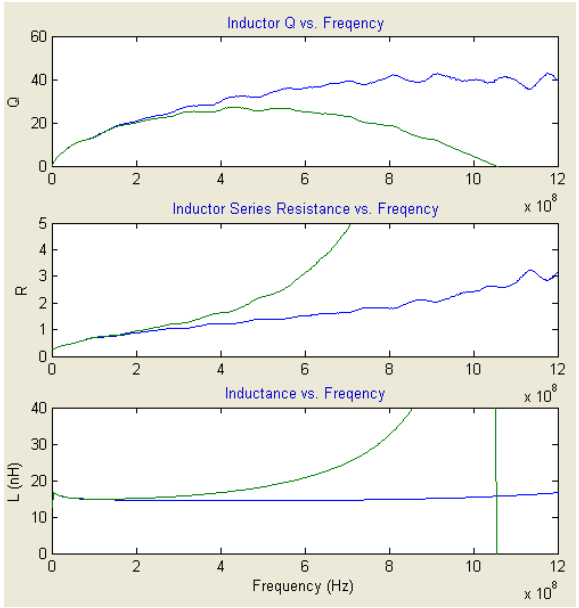




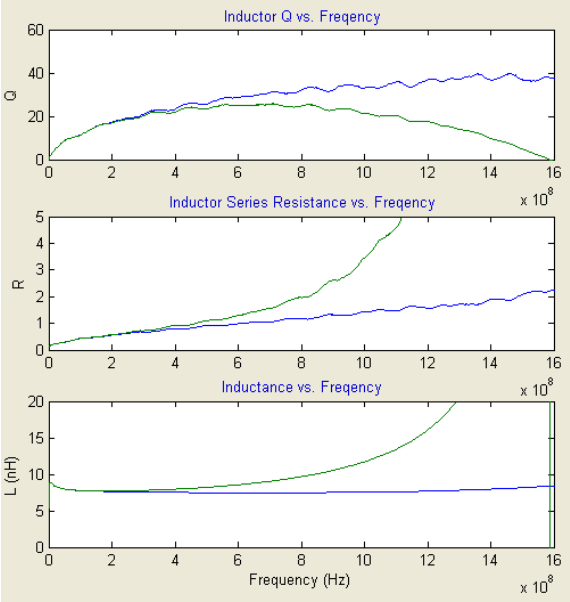
H1: 3 turns, 12mil pitch, .5dia shield width, 1dia shield length



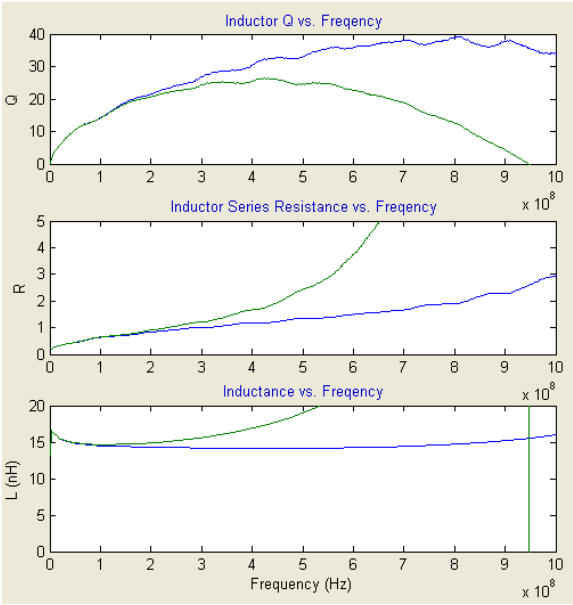
H3: 6 turns, 12mil pitch, 1dia shield width, 2dia shield length



H4: 3 TURNS, 18MIL PITCH, .5DIA SHIELD WIDTH, 1DIA SHIELD LENGTH

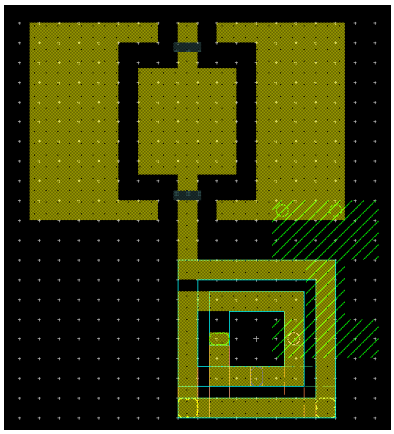


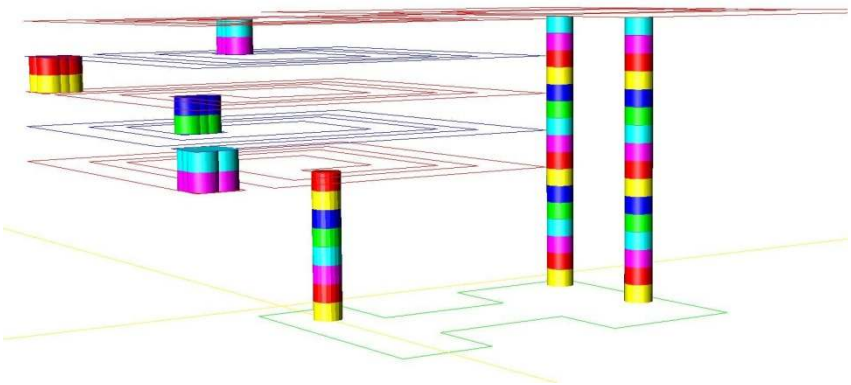
H5: 6 TURNS, 18MIL PITCH, .5DIA SHIELD WIDTH, 1DIA SHIELD LENGTH



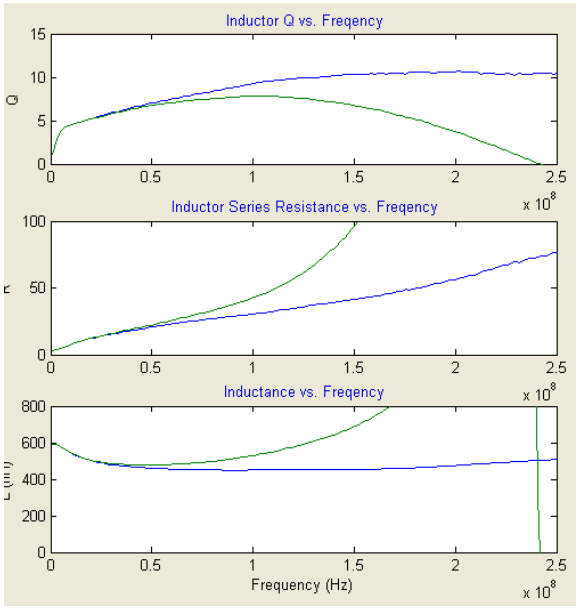
K: Flat Spirals

In order to compare the performance of FTTF solenoids, a selection of similarly-sized spiral inductors were included. These spirals are printed in the flat metal and are connected by traditional vias. The spirals are all identical and have 2 turns. Spirals on different layers are connected one of three ways; series, parallel, or tied stacked. In series, the top inductor spirals in. A via connects to the next spiral which is rotated so that it spirals back out and maintains direction. Using this technique, a great many turns can be packed into a small area. The parallel structures are several spirals connected with vias at the outside and inside of the spiral. The stacked spirals are like the parallel structures, but have vias tying them together at each point where the spiral changes direction. The intention for this was to emulate a spiral inductor made with FTTF. As previously mentioned, a spiral made with FTTF would be difficult because the tape in the center would not be sufficiently supported. This was achieved, however, in [15]. This was done by cutting the green tape with a laser after it has been laminated with another layer of green tape.

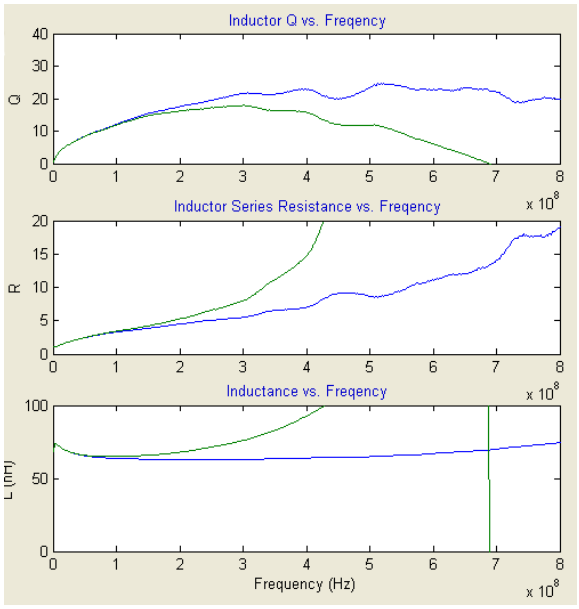




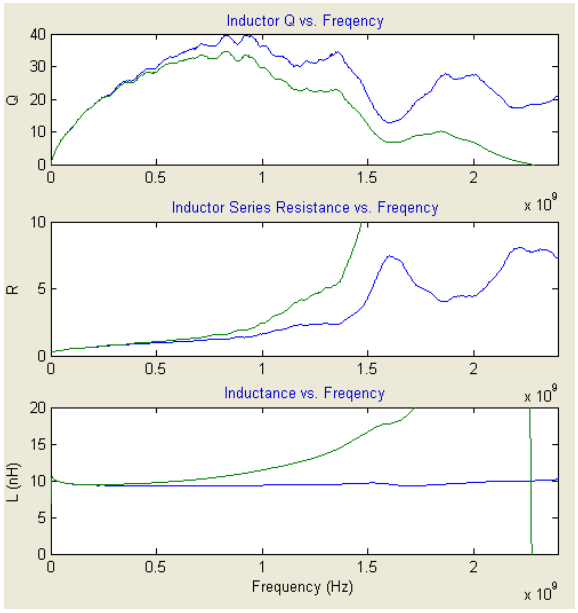
K1: 15 layers, series



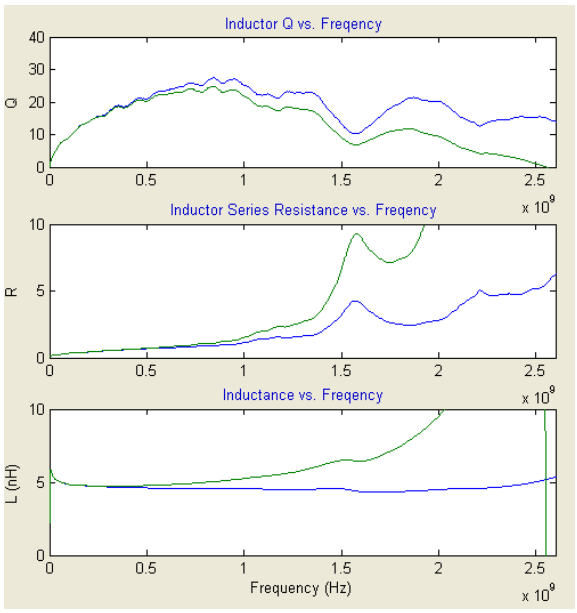
K2: 5 layers, series



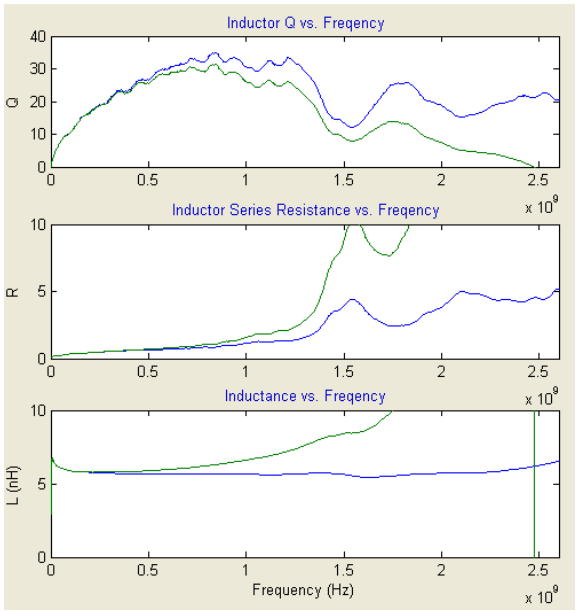
K3: 1 LAYER (SINGLE SPIRAL)



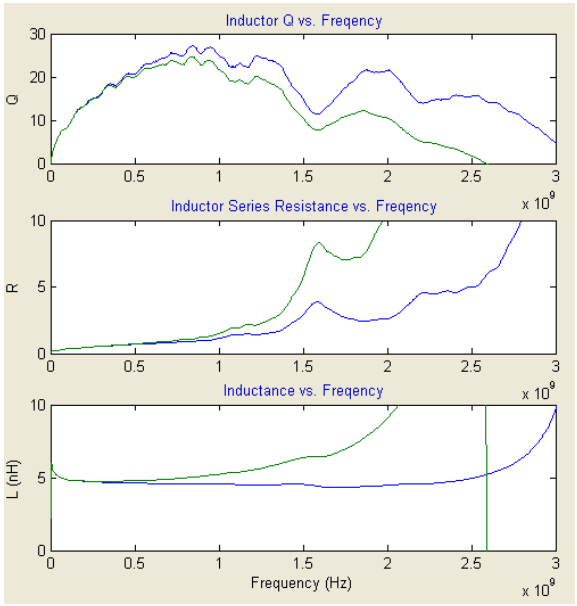
K4: 15 LAYERS, PARALLEL



K5: 5 LAYERS, PARALLEL



K6: 15 LAYERS, STACKED



K7: 5 LAYERS, STACKED