A Fully Integrated UHF CMOS Power Amplifier for Spacecraft Applications

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***Abstract*—A power amplifier (PA) is designed for a surface-to-orbit proximity link microtransceiver on Mars exploration rovers, aerobots, and small networked landers and works in conjunction with a 0.2-dB loss transmit/receive switch to allow nearly the full 1 W to reach the antenna. The fully integrated UHF CMOS PA with more than 30-dBm output is reported for the first time. A differential pMOS structure with floating-bias cascode transistors and 1 : 3-turn ratio output transformer are chosen to overcome low breakdown voltage ($V_{\rm bk}$) of CMOS and chip area consumption issues at UHF frequencies. The high-Q on-chip transformer on a sapphire substrate enables the differential PA to drive a single-ended antenna effectively at 400 MHz. The PA in a standard package delivers 30-dBm output with 27% power-added efficiency. No performance degradation was observed in continuous-wave operation and the design has been tested to 136% of its nominal 3.3-V supply without failure.**

***Index Terms*—CMOS, power amplifiers (PAs), transceiver, transformer, transmit/receive (TR) switch.**

I. Introduction

In JANUARY 2004, photographic panoramas from another world were transmitted to Earth by the Mars Exploration Rovers, Spirit and Opportunity, captivating the public's attention. In the following year, more than 90 Gbits of photographs and data were relayed through the UHF surface-to-orbiter proximity links [1], offering evidence of past liquid water environments in which life could have developed.

Despite their great scientific functionality and achievements, the rover's large size ($\sim$5 m^3) and mass ($\sim$185 Kg) allowed only one rover per launch, limiting surface exploration of the planet to only two sites [2]. If a number of much smaller scout vehicles could be designed, the number of successful missions at given revenue would increase dramatically and many more sites could be explored. The Mars microtransceiver project, under which this study was carried out, targets significant reductions in size, mass, and power consumption of the UHF communications radio system as an enabling technology for such future missions [3].

Although reduction of a radio communication circuit's size/mass comes directly from high integration, the associated power amplifier (PA) is implemented traditionally in a compound semiconductor process and requires additional off-chip components. A fully integrated CMOS PA would let a miniature transceiver unit be built with two analog chips, one digital chip, and a few off-chip parts, as illustrated in Fig. 1 [3], [4]. Moreover, an integrated UHF-band PA opens the possibility for a single-chip microtransceiver implemented entirely in the space-qualified silicon-on-sapphire (SOS) CMOS process selected for this study.

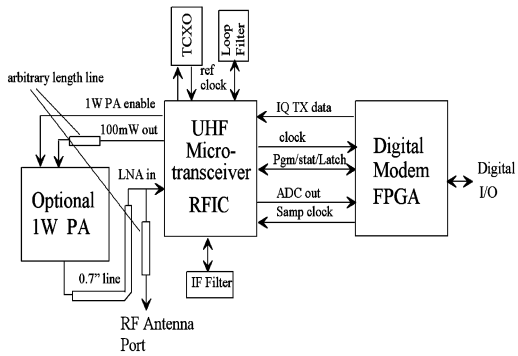

Fig. 1. Microtransceiver layout floor plan. From [4].

Efforts to build a watt-level CMOS PA can be found in numerous papers. 1-W output has been successfully demonstrated in the 1.9-GHz cellular frequency band in [5]. However, due to the lossy silicon substrate, bond-wire inductances and an off-chip microstrip-line balun were utilized. A similar level of performance was also achieved in a single-ended structure at 1.8 GHz with comparable use of off-chip components [6]. Yoo and Hwang have shown that a common-gate switching technique can avoid the CMOS's low voltage breakdown problem in the 900-MHz 0.9-W PA [7] and a very high-efficiency fully differential PA was reported by Mertens and Steyaert [8]. However, both have to depend on off-chip circuit components or be forced to interface a differential antenna nearby in the absence of a high-quality inductor/balun.

A fully integrated 2.4-GHz 2.2-W CMOS PA was reported by Aoki *et al.* where a distributed active transformer (DAT) combines outputs of circularly laid-out differential pairs [9]. The DAT technique fits well for the 2.4-GHz application, but the Mars transceiver's much lower operating frequency (400 MHz at TX, 435 MHz at RX) makes it impossible to fit such a PA on a 3×3 mm^2 die.

This paper describes challenges in CMOS integration of watt-level PAs at UHF in Section II and their solution and improvements by new design techniques such as using high $V_{\rm bk}$ p-channel devices and a 1 : 3 ratio on-chip transformer in Section III. The companion TR switch function is addressed in Section IV. Measurements are then summarized in Section V followed by conclusions in Section VI.

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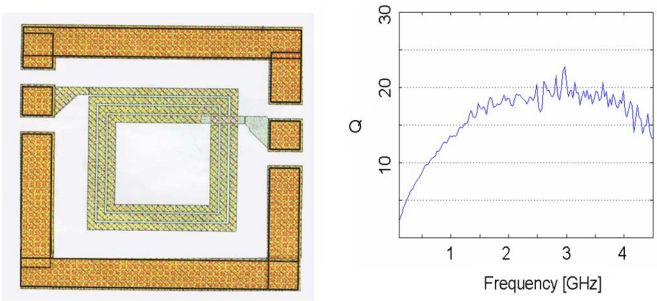

(a) (b)

Fig. 2. Spiral inductor in SOS. (a) Test structure of a $450 \times 450\ \mu\text{m}^2$ inductor. (b) Q plot.

II. Fully Integrated CMOS PA: Challenges

A fully integrated watt-level CMOS RF PA has been a formidable task due to barriers given by CMOS processes. In order to deliver higher output power, the net size of the transistors must increase proportionally. Since CMOS does not have as much gain as GaAs, very wide gates are needed and associated large gate capacitance becomes hard to match. Moreover, when multiple transistor cells are used, parasitic inductance and resistance in gate and source distribution networks drop capacitive input Q, effectively increasing input conductance. Similar problems are found when bond-wire parasitics are considered, such that many designs have moved toward differential structures.

For watt-level output at a 50-Ω load, voltage swing should be larger than 10 V_{peak}. GaAs and LDMOS can handle much higher drain–source voltage than CMOS and multiwatt PAs have been reported without extra efforts to reduce the drain voltage swing in these processes [10]–[12]. However, CMOS transistors will be broken by the stress in the same circuit. Therefore, cascoding, output transformation to increase output voltage, and/or combinations of multiple outputs are required.

Stability issues must also be considered. Since PAs create a variety of input/output feedback paths through magnetic coupling, and transistor parasitic capacitance and signal levels are very large, careful layout and modeling are essential before fabrication. Finally, heat dissipation in the PA is hard to simulate in advance due to the concentration of heat at the transistor channel regions. If we assume a fully integrated PA has 50% drain efficiency (DE) and 1-W output, which is not very easy in CMOS, the PA must dissipate 1 W as heat, spreading it away from the transistor drains as efficiently as possible since temperature increase in the devices results in carrier mobility reduction and degrades overall performance.

Whereas innovative design strategies are needed to address many of the aforementioned challenges, some of them can be relieved by using an RF-aware CMOS process. In this project, SOS is used due to its potential for high-quality inductors [13]. As shown in Fig. 2, the maximum Q of a 3.25-turn inductor is close to 20 at S-band and can exceed 10 at UHF, which is approximately twice as high as that of the inductor on a silicon substrate with similar dimensions [13], [14]. In addition, its radiation hardness is well suited in the Mars application [15].

III. PMOS Cascoded Differential Class-E PA Design

Designing RF PAs involves close attention to efficiency, signal swings, device breakdown, and resonant circuit Q.

A. Selection of PA Class for Good Efficiency

In the absence of complex linearization systems, linearity is often sought using a class-AB mode design. RF CMOS class-AB PAs have reported around 30% power-added efficiency (PAE) with satisfactory linearity for their application objectives [16]–[18]. Yet, there are additional nonlinear mode PAs like class-D, class-E, class-F, and so on, which may be applicable for certain modulation types—notably Gaussian minimum shift keying (GMSK). In these modes, the transistors act as either switches or saturated current sources and the output power is not proportional to the input power—instead it is a function of power-supply voltage. By giving up linear input/output relations, these PAs can convert all the dc power into RF output power theoretically and they are suitable for systems with constant amplitude modulation such as GMSK and unfiltered binary phase-shift keying (BPSK), quadrature phase-shift keying (QPSK), and residual-carrier BPSK used in spacecraft systems. Space systems based on the Proximity-1 Space Link Protocol [19] have relaxed linearity requirements. Thus, a nonlinear mode PA is the focus of this paper.

Although PAs using nonlinear modes can acquire a theoretical 100% efficiency, practical limitations keep the efficiency well below perfection. For example, the class-D mode has rarely been implemented in RF CMOS because its finite switch transition time and parasitic capacitance results in high drain voltage and current product [20]. The multiharmonic tuned class-F mode is not practical since the additional on-chip harmonic resonators involve more loss rather than increasing the efficiency. However, the class-E mode was invented originally for no switch transition loss and needs only one resonator at its output network. Moreover, a differentially driven class-E with a finite RF choke inductor has extra advantages such as less sensitivity to bond-wire parasitics, good even-order harmonic rejection, and low resistive loss across the RF choke inductor [9], [11].

In this paper, we choose the cascoded differential class-E mode for high efficiency and reproducibility. A watt-level output PA is realized without violating breakdown voltage (V_{bk}) limit through the use of pMOS devices with high V_{bk}, cascode differential switching, and an on-chip 1 : 3 ratio transformer, as shown in Fig. 3.

B. Signal Swing and Breakdown Issues

As a CMOS process scales, its drain–source V_{bk} tends to scale. For example, at 0.35 μm, transistors may break down at around 4 V, while at 0.18 μm, devices would fail at only 2 V. Fortunately, in the selected SOS process, good high-frequency performance exceeding that of 0.35-μm bulk CMOS is achieved at 0.5 μm [15]. Moreover, measurements indicate that the pMOS transistor V_{bk} is well above 4 V in the targeted SOS process, as shown in Fig. 4. Although the high V_{bk} of the pMOS device is traded with lower transconductance and higher switch resistance, the DE of the PA can still improve with higher power supply. In an ideal class-E PA, maximum drain voltage

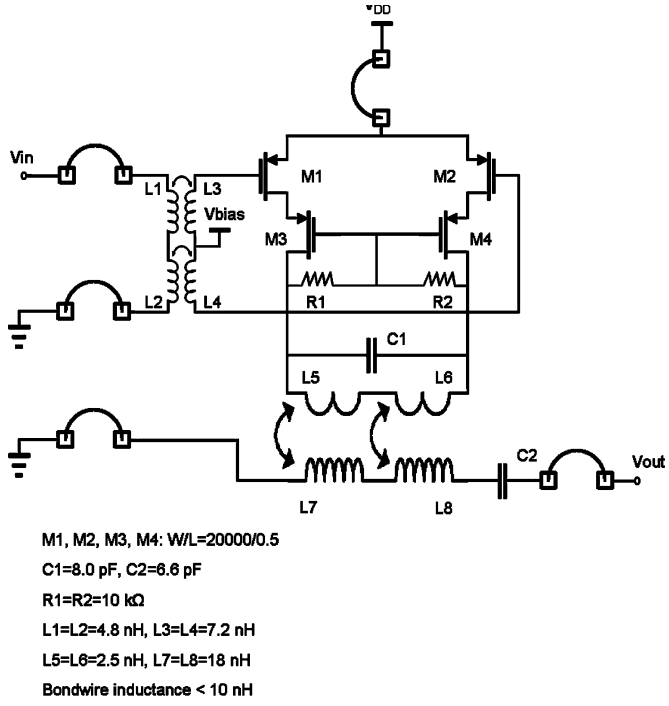

Fig. 3. Cascoded differential class-E PA schematics. Inductance and coupling coefficient are extracted from an electromagnetic simulator ($k_{L1,L3} = k_{L2,L4} = 0.73$ and $k_{L5,L7} = k_{L6,L8} = 0.75$).

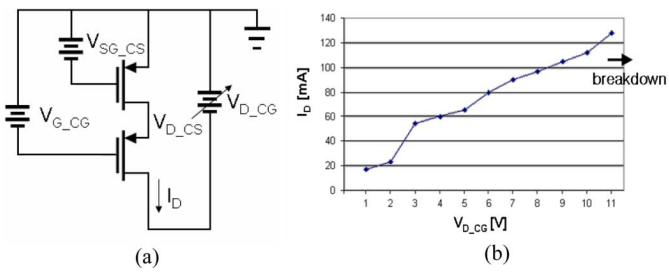

Fig. 4. pMOS cascode transistors $V_{\rm bk}$ test. (a) Schematics. $V_{\rm SG\_CS} = V_{\rm TH} + 0.05\,{\rm V} = 0.3\,{\rm V}$, $V_{G\_\rm CG} = 3.3\,{\rm V}$, and W/L $= 20000/0.5$. (b) I_D versus $V_{D\_\rm CG}$ plot.

$(v_{D,\max})$ is 3.56 $V_{\rm DD}$. At the maximum voltage, if the MOSFET threshold $V_{\rm TH}$ is much less than $V_{\rm DD}$, source–drain voltage of the common-source transistor $(v_{\rm SD\_CS})$ levels off at $V_{\rm DD}$ and source–drain voltage of the common-gate transistor $(v_{\rm SD\_CG})$ rises up to 2.56 $V_{\rm DD}$, which must be less than $V_{\rm bk}$ in the cascoded class-E PA [7]

$$v_{D,\max} = 3.56V_{\rm DD} = v_{\rm SD\_CS} + v_{\rm SD\_CG} = V_{\rm DD} + V_{\rm bk}. \quad (1)$$

Hence, the required breakdown voltage is

$$V_{\rm bk} < 2.56V_{\rm DD}. \quad (2)$$

When $V_{\rm DD}$ is set for the process limit $(V_{\rm DD} = V_{\rm bk}/2.56V)$, output power is [21]

$$P_o = 0.577\frac{V_{\rm DD}^2}{R} = 0.577\left(\frac{V_{\rm bk}}{2.56}\right)^2\frac{1}{R} \quad (3)$$

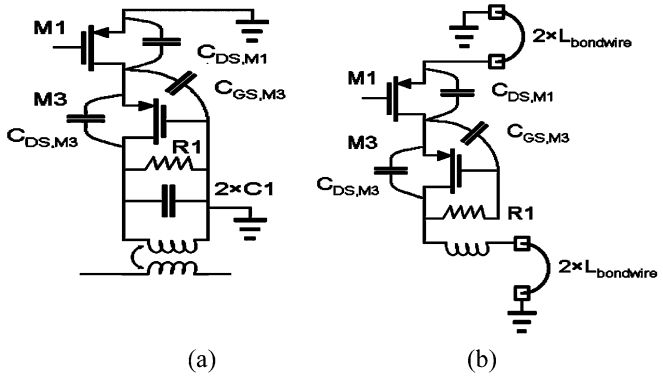

Fig. 5. Half circuit schematics: (a) at fundamental and odd harmonics and (b) at even harmonics.

where R is load resistance

$$R = 0.577\left(\frac{V_{\rm bk}}{2.56}\right)^2\frac{1}{P_o}. \quad (4)$$

Efficiency of the class-E PA with switch on-resistance $(R_{\rm on})$ loss [21] $P_{R\rm on}$ is found as function of $R_{\rm on}$ and $V_{\rm bk}$ by substituting R with (4) as follows:

$$\eta_{R_{\rm on}} = \frac{P_o}{P_o + P_{R_{\rm on}}} = \frac{R}{R + 1.365R_{\rm on}} \approx \frac{1}{1 + \dfrac{15.5R_{\rm on}P_o}{V_{\rm bk}^2}}. \quad (5)$$

Since the high $V_{\rm bk}$ allows high R, the efficiency reduction by the high $R_{\rm on}$ of the p-channel device is compensated by the high $V_{\rm bk}$. For example, an nMOS class-E PA with $R_{\rm on} = 0.5\ \Omega$ and $V_{\rm bk} = 4$ V has 67% $\eta_{R\rm on}$ for 1-W output. When pMOS has $R_{\rm on} = 1\ \Omega$ and $V_{\rm bk} = 9$ V, the pMOS class-E PA has $\eta_{R\rm on}$ of 83% despite its larger $R_{\rm on}$. The pMOS devices, therefore, form the core of the PA design in this application and the added voltage swing afforded by them is leveraged to achieve the desired 1-W output on a single 3.3-V supply.

The schematic of the implemented pMOS cascoded differential class-E PA is shown in Fig. 3. The differential structure provides a near virtual ground to the common-source stage, mitigating gain reduction by bond-wire inductive degeneration. The virtual ground at the output keeps the RF currents in the primary coil from entering the GND bond wire, improving immunity of the design to bond-wire inductance.

The pMOS differential pairs are cascoded to allow high voltage swing at the primary and the common-gate transistors are self-biased by a resistor voltage divider without extra bond-wire connection to ground. Large R1 and R2 have little effect on the load circuit at the fundamental and odd harmonics and a virtual ground develops at the common-gate, as shown in Fig. 5(a). At the even harmonics, the primary currents both flow to the center-tap, and no voltage or current is developed in the secondary coil and a virtual open circuit is achieved between M3 and M4. Hence, the drain of M1 sees very high impedance toward the transformer leaving $C_{\rm DS,M1}$ as the dominant load effectively, as shown in Fig. 5(b). Thus, the self-bias enables cascoded switching without altering the differential class-E performance.

Measurements of the pMOS cascode test structure in Fig. 4 show that the pMOS cascode transistors break down at $V_{D\_CG} = 12$ V when V_{G_CG} is fixed at 3.3 V. Since V_{SD_CS} is approximately 3 V with low V_{TH} and negligible overdrive voltage ($V_{TH} + \Delta V \approx 0.3$ V), the V_{bk} of pMOS is 9 V. However, we limit v_{SD} not to exceed 5 V for reliability since the voltage swing is also limited by oxide breakdown voltage, which is approximately 6–7 V for 100-Å-thick oxide [22]. It should be noted that the pMOS used here is not specially manufactured to achieve the high breakdown performance. The performance shown in Fig. 4 is that of standard device in the 0.5-μm FC (mixed-signal/RF process with thick tip metal layer and metal–insulator–metal (MIM) capacitor options) peregrine process.

C. Transformer Design

In this design, the output transformer converts 50-Ω load resistance into differential 10 Ω and tunes output impedance for the class-E mode, requiring a non-1 : 1-turn ratio. On-chip transformers have low coupling between primary and secondary coils and, therefore, the resistance transform ratio does not follow turn ratios quadratically [14]. In order to predict the transformer behavior accurately, the Agilent Momentum electromagnetic simulator was used. Considering power loss and imperfect coupling, 1 : 3-turn ratio is chosen for 1-W output. The transformer (L5–L8) has $Q_p = 10, Q_s = 13$ and coupling coefficient $k = 0.75$ in simulation. The transformer efficiency (η_T), calculated by (6) [23], is 79%

$$\eta_T = \frac{1}{1 + 2\sqrt{(1+A)A} + 2A}$$
$$A = \frac{1}{Q_p Q_s k^2}. \tag{6}$$

For comparison, a Q of 5 for a transformer on the bulk CMOS process, which is not an underestimated value at 400 MHz [14], results in 59% efficiency by the same equation (6).

Two transformers are used for the input balun (L1–L4) and they are wound in opposite directions to minimize the effects of magnetic coupling to the output transformer. Otherwise the coupling would degrade performance and could cause instability. These transformers are smaller in size with resulting lower Q and efficiency, but are less critical in the overall amplifier efficiency result.

D. Power Loss and Efficiency of PA Core

The power loss of the PA core is composed of switch loss ($P_{R\text{on}}$), capacitive loss (P_C), and current turn-off time loss (P_{off}). The total power loss can be estimated by computing each power loss contributor under ideal conditions and summing them [24].

By rearranging (5), the power loss in the half circuit of Fig. 5 due to R_{on} at 50% duty cycle operation is

$$P_{R_{\text{on}}} = 1.365 \frac{R_{\text{on}}}{R} P_o \tag{7}$$

where $R_{\text{on}} = R_{\text{on,CS}} + R_{\text{on,CG}}$ and R is single-ended load resistance.

Although class-E topology avoids capacitive loss by doing zero voltage switching (ZVS), the common-source output (v_{SD_CS}) is not shaped for the ZVS and the drain capacitance of the common-source must be charged and discharged every cycle without contributing output power

$$P_C = C_D (V_{DD} - V_{TH} - V_{\text{on}})^2 f \tag{8}$$
$$C_D = C_{\text{DS,M1}} + C_{GS\cdot M3} + C'_{\text{GD},M1} \tag{9}$$
$$V_{\text{on}} = \frac{1.365 R_{\text{on}}}{R + 1.365 R_{\text{on}}} V_{DD} \tag{10}$$

where C_D is capacitance at the drain, $C'_{\text{GD},M1}$ is effective gate–drain capacitance by Miller's effects, and V_{on} is the common-source switch voltage by $R_{\text{on,CS}}$ and i_D. Equation (8) is rewritten as function of P_o and substituting $1.73 P_o R$ for V_{DD}^2 by (3), yielding

$$P_C = C_D \left(1 - c_1 - \frac{1.365 R_{\text{on,CS}}}{R + 1.365 R_{\text{on,CS}}}\right)^2 V_{DD}^2 f$$
$$= 1.73 C_D \left(1 - c_1 - \frac{1.365 R_{\text{on,CS}}}{R + 1.365 R_{\text{on,CS}}}\right)^2 P_o R f \tag{11}$$

where

$$c_1 = V_{TH}/V_{DD}. \tag{12}$$

The current turn-off time loss is approximated as [24]

$$P_{\text{off}} = \frac{1}{12} \tau_f^2 P_o. \tag{13}$$

The τ_f is turn-off time in radians.

Finally, the efficiency of the PA core is approximated by

$$\eta_{\text{core}} = \frac{P_o}{P_o + P_{R_{\text{on}}} + P_C + P_{\text{off}}}. \tag{14}$$

Since the PA is not tuned for infinite number of harmonics due to low output resonant circuit Q, the nominal efficiency (η_{nom}) is assumed to be that of a second and third harmonics tuned class-E PA (80%) [25]. Consequently, the total efficiency is

$$\eta_{\text{total}} = \eta_{\text{nom}} \times \eta_{\text{core}} \times \eta_T. \tag{15}$$

By substituting the parameters for this design where $R_{\text{on,CS}} = 0.55\ \Omega, R_{\text{on,CG}} = 0.33\ \Omega, C_D = 50$ pF, and $\tau_f = 2\pi/5$, the power losses are $P_{R\text{on}} = 0.24 P_o, P_C = 0.11 P_o$, and $P_{\text{off}} = 0.13 P_o$, resulting in $\eta_{\text{core}} = 68\%$. Hence, η_{total} is approximately 44%.

IV. TR Switch Function

It has been suggested that a traditional GaAs TR switch can be replaced by an integrated resonant TR switch [26], although experimental results were only provided for the low-noise amplifier (LNA) input protection side of the required SPDT switch. Reference [26] shows that the resonant TR switch can protect an LNA in the 3-V process from up to 5-W PA output. Reference [27] illustrated that the resonant TR switch concept can be integrated into the PA also at up to the 100-mW level, and a fully integrated transceiver RF front-end is implemented. With proper

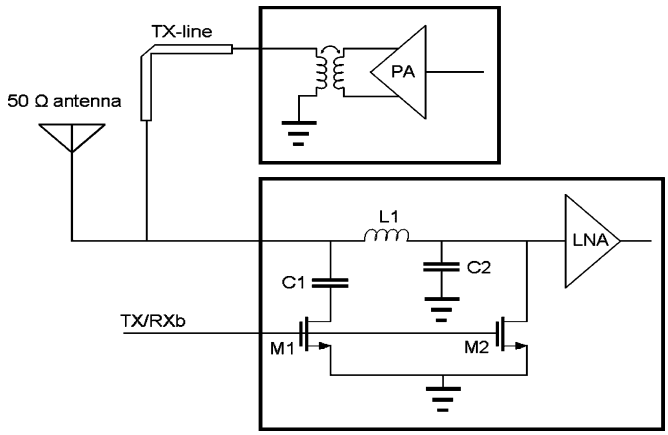

Fig. 6. Resonant TR switch at the LNA and the PA output transformation by transmission line.

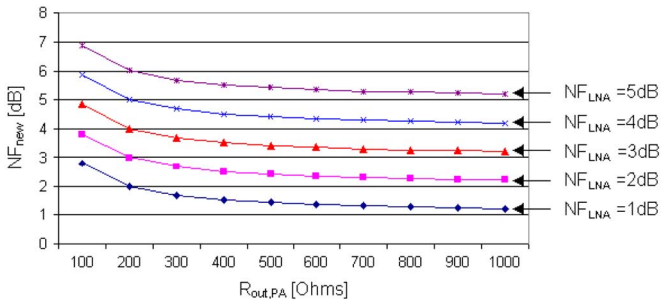

Fig. 7. NF degradation due to the PA output resistance. $\mathrm{NF}_{\mathrm{new}}$ is the degraded NF from $\mathrm{NF}_{\mathrm{LNA}}$.

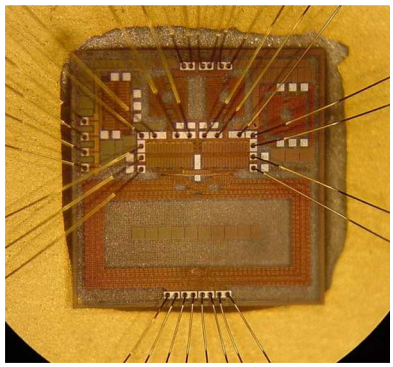

Fig. 8. Die microphotograph of the PA with bond wires.

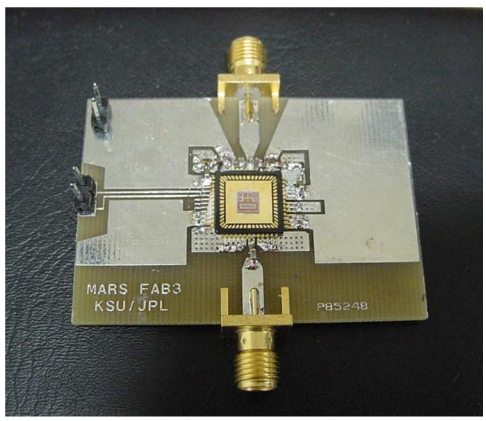

Fig. 9. Test board. Bypass capacitors near the package and one tuning capacitor at the output are used.

design, the LNA's input resistance is raised to 1 kΩ during the transmit operation and absorbs only 0.2 dB of the PA's output power, yielding excellent overall efficiency. Reference [27] also shows that high resistance output from the PA at the receive mode limits degradation of the receiver noise figure (NF) to a negligible value for the 100-mW PA case.

In the current 1-W PA design covered in this paper, these techniques are employed to provide a full TR function, as shown in Fig. 6. In the transmit mode, the TX/RXb control signal shorts the LNA input to ground and L1–C1 parallel tank presents high impedance toward the antenna. Assuming a 50-Ω antenna and $Z_{\mathrm{in,LNA}} \gg R_{\mathrm{ant}}$, most of the power from the PA is radiated through the antenna with little loss. The loss by the switch can be derived as

$$\frac{P_{\mathrm{loss}}}{P_{\mathrm{out}}} = \frac{V_{\mathrm{ant}}^2/R_{\mathrm{in,LNA}}}{V_{\mathrm{ant}}^2/(R_{\mathrm{in,LNA}} \| R_{\mathrm{ant}})}. \tag{16}$$

When the LNA is implemented to provide a 1-kΩ reflective termination during transmit, the $P_{\mathrm{loss}}/P_{\mathrm{out}}$ can be held less than 5% (0.2-dB loss) [27].

At the receive mode, all the transistors in the PA are shut down and output impedance at the PA chip is inductive due to the secondary output coil. If the LNA sees very high impedance toward the PA output through suitable resonating capacitance or transmission line angle rotations, signal-to-noise ratio at the input is affected minimally. Although the PA output is not resonant at the 435-MHz receive frequency, a short length of transmission line can be added to bring the impedance to a high value. Thus, the NF of the LNA $(\mathrm{NF}_{\mathrm{LNA}})$ is not significantly degraded. For instance, when an LNA with 3-dB NF is combined with a PA, which presents 400-Ω resistance toward the LNA, the resultant NF $(\mathrm{NF}_{\mathrm{NEW}})$ is 3.5 dB, as shown in Fig. 7. The NF calculation is detailed in the Appendix, and the additional issue of noise generation in the PA during the receive mode is covered in Section V.

V. Implementation and Measurements

The PA is fabricated in a 0.5-μm Peregrine SOS and the die size is 3.2×3.2 mm^2. A 52-pin standard package and FR4 printed circuit board (PCB) are used to build a test board. The die microphotograph and the test board photograph are shown in Figs. 8 and 9, respectively. All the metal layers carrying large rms current are drawn obeying electromigration rules. The PA has strong immunity to bond-wire parasitics, as previously explained, allowing it to be placed in the package instead of chip-on-board. Hence, a gold-plated PCB is not necessary for the work. Fourteen bond wires to power supply and ten bond wires to ground are connected around the package and are spaced in order to decrease source resistance and mutual inductance among the bond wires. A 4.7-pF surface mount capacitor is added in series at the output to adjust output network, but this can easily be moved into the chip in the next version.

Fig. 10 shows the PA's output power and PAE with input power variation. It is originally designed for 20-dBm input coming from a separate microtransceiver chip [3], [27]. When

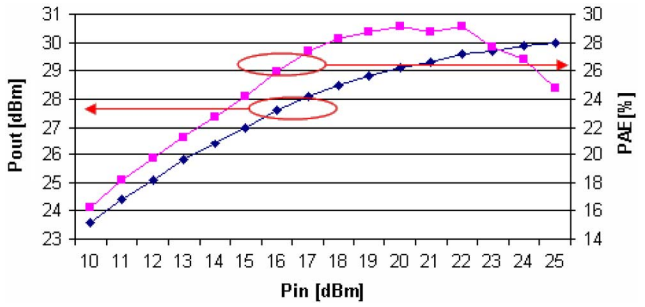

Fig. 10. P_{out} and PAE with P_{in} variation.

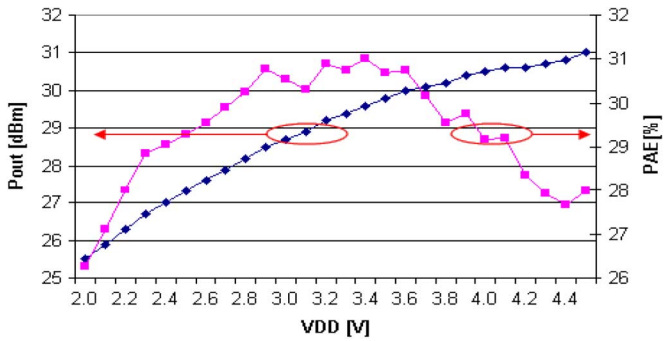

Fig. 11. P_{out} and PAE with fixed 20-dBm P_{in} and power-supply variation.

the PA is driven by the transceiver, 29 dBm $P_{\rm out}$ and 29% PAE are measured at 3.3-V dc. Its DE is 33%. The difference from the calculated efficiency predicted by (15) is ascribed to imperfect tuning, modeling inaccuracy, and transformer asymmetry. 30-dBm output is achieved with 24-dBm input with 27% PAE. Output power is also measured over power-supply variation. As shown in Fig. 11, the output power monotonically increases up to 31 dBm at $V_{\rm DD} = 4.5$ V. Since the input gate bias was not adjustable for the best efficiency during this measurement, the highest PAE is found at 3.3 V where the PA is optimized.

While increasing the power-supply voltage, time-domain waveforms at drains of cascoded pairs are probed in order to observe $v_{\rm SD}$ stress. A 1 : 100 needle probe was used and the probed signal was passed through a 6-dB resistive power splitter to trigger a 20-GHz oscilloscope (HP 83480A). Fig. 12 shows that $v_{\rm SD}$ is 5 V for the common-source pair and $V_{\rm peak}$ at the primary coil is approximately 7.5 V at $V_{\rm DD} = 3.3$ V. Waveforms at $V_{\rm DD} = 4.5$ V are also shown in Fig. 13. While the self-biased cascoded pairs generate 31-dBm output, the maximum $v_{\rm SD}$ stress is 6 V with 4.5-V power supply. The waveforms do not match optimum class-E's because the output parallel tank has low $Q(\approx 1)$ to reduce transformer loss, which makes harmonic tuning imperfect. The difference between the simulation and measurements are believed to be from inaccurate modeling of parasitic $C_{\rm DS}$. No performance setback was observed in continuous operation of the amplifier at 4.5 V.

Frequency response is shown in Fig. 14. At the fixed 20-dBm input power, the PA has very wide bandwidth, approximately 200 MHz, due to low resonance circuit Q at the output network. The output impedance is measured. When transmission line delay is added into vector network analyzer (HP 8753E) calibration, the output impedance is approximately 360 Ω (Fig. 15).

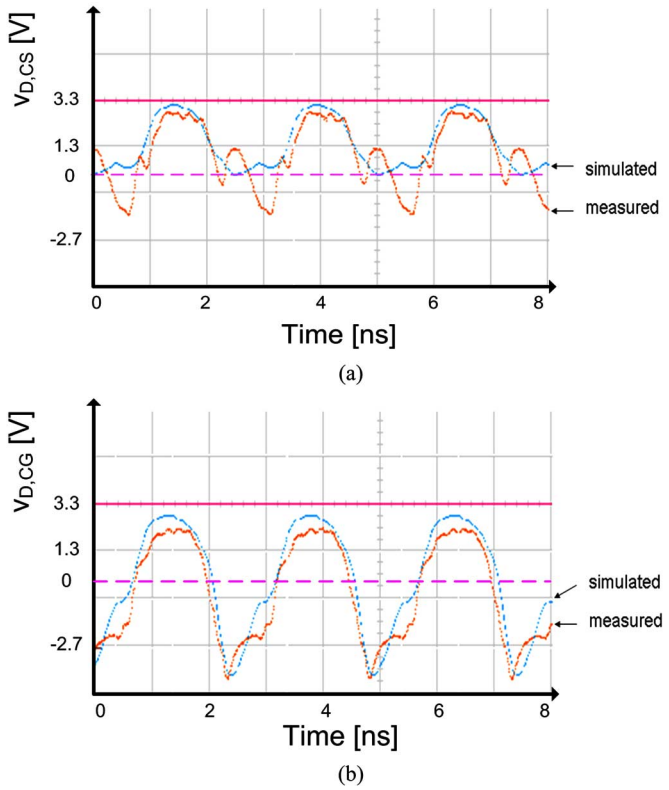

Fig. 12. Drain voltage waveforms of: (a) common source pair and (b) common gate pair with 3.3-V power supply.

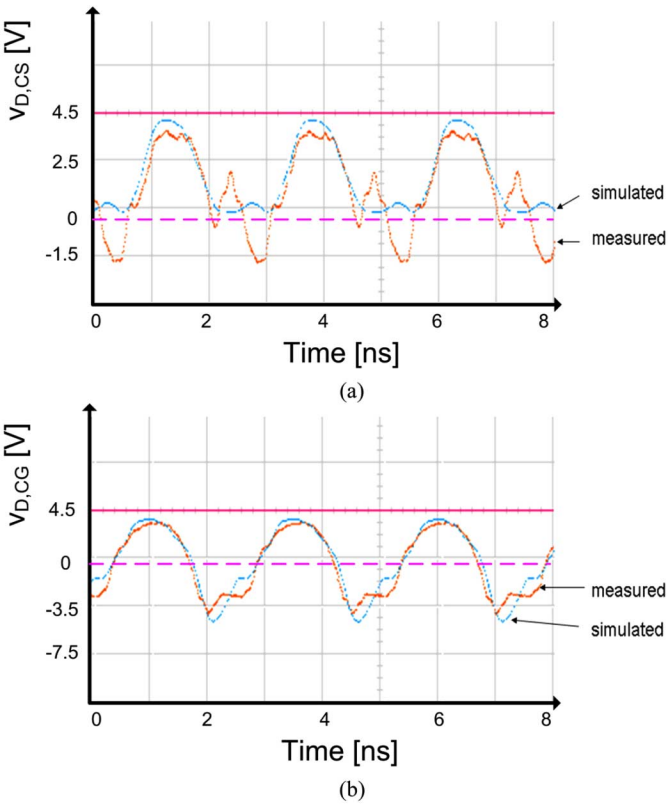

Fig. 13. Drain voltage waveforms of: (a) common source pair and (b) common gate pair with 4.5-V power supply.

From (A.9), this is equivalent to 0.6-dB degradation in the NF. Finally, off-state noise contribution of the PA is also measured.

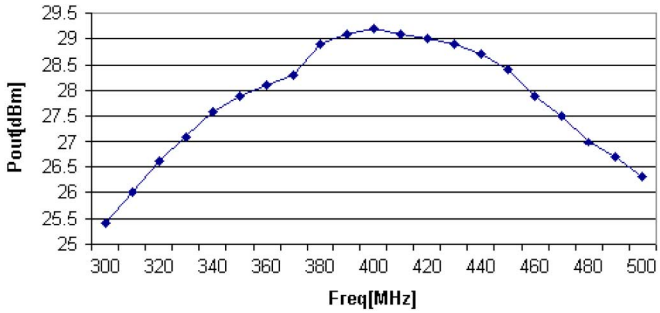

Fig. 14. Frequency response with fixed 20-dBm $P_{\rm in}$.

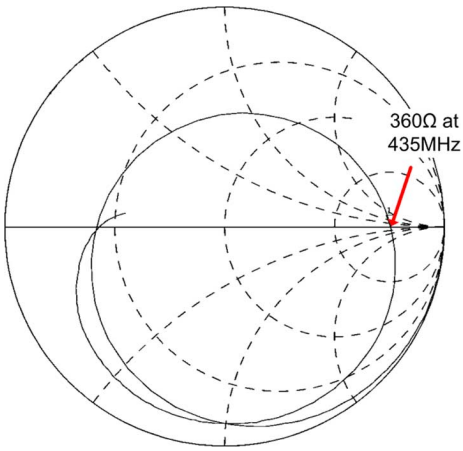

Fig. 15. Output impedance measured at receive mode with −125-ps reference plane extension.

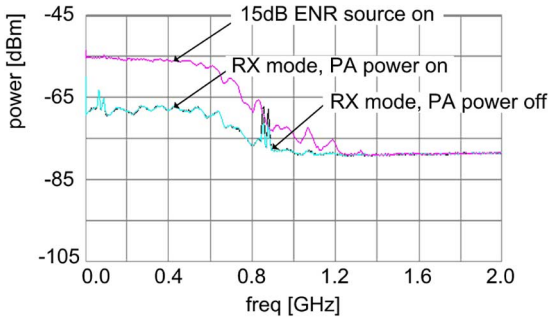

Fig. 16. Output noise measured with a 40-dB gain LNA before the spectrum analyzer. Turning on power supply does not increase the noise floor at RX mode. Thus, PA power on and off plots overlap.

The PA's output is amplified by a 40-dB LNA (HP 8447A) before it is connected to a spectrum analyzer (Agilent E4402B). As shown in Fig. 16, no noise floor increase is observed when the power supply is turned on. A spectrum with a 15-dB excess noise ratio (ENR) source input is also displayed to validate that the test setup is sufficiently sensitive to detect any noise increase that would affect the 3-dB system NF of the microtransceiver.

VI. Conclusion

A fully integrated watt-level CMOS PA has been a tough hurdle to overcome due to the process' digital-oriented characteristics. Although some successful PAs have been reported, many depend on off-chip components such as bond wires and transmission lines, while others are not easily scaled to lower frequencies. In order to achieve high repeatability and pursue a single chip radio, the off-chip components cannot be used. This study has demonstrated a fully integrated UHF CMOS PA in a CMOS SOS process. High $V_{\rm bk}$ pMOS transistors are cascoded instead of nMOS to stand high drain voltage. In addition, a 1 : 3-turn ratio transformer/balun on the SOS process converts a single-ended load resistance to a lower differential resistance with high efficiency. Using both techniques, watt-level output is delivered without multiple PAs' output combining, off-chip output matching network, and a balun. The PA in a standard package delivers 29 dBm with 29% PAE at 20-dBm input and 3.3-V power supply. Over 30-dBm output with lower PAE is also measured either with higher input power or higher power supply. It can also be combined with the resonant TR switch without significant NF degradation at the receive mode. To the authors' knowledge, the PA is the first fully integrated UHF CMOS 1-W PA in the standard package.

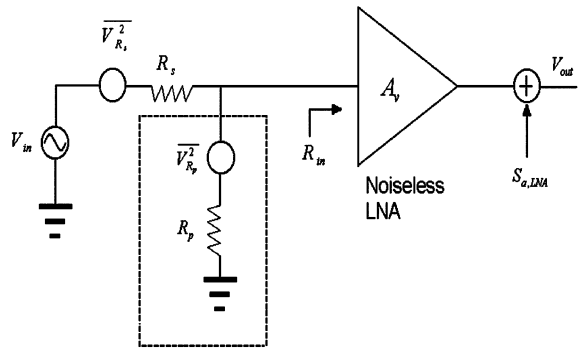

Fig. 17. Noise model of the TR switch. Added noise $S_{a,\rm LNA}$ is separated from the ideal LNA.

Appendix
NF Calculation

The NF of an LNA before a PA is attached can be calculated directly from Fig. 17 excluding the dotted box. The results are

$$\left(\frac{S_i}{N_i}\right)_{\rm LNA} = \frac{V_{\rm in}^2\left(\dfrac{R_{\rm in}}{R_s+R_{\rm in}}\right)^2}{\overline{V_{R_s}^2}\left(\dfrac{R_{\rm in}}{R_s+R_{\rm in}}\right)^2} \tag{A.1}$$

$$\left(\frac{S_o}{N_o}\right)_{\rm LNA} = \frac{V_{\rm in}^2\left(\dfrac{R_{\rm in}}{R_s+R_{\rm in}}\right)^2 A_v^2}{\overline{V_{R_s}^2}\left(\dfrac{R_{\rm in}}{R_s+R_{\rm in}}\right)^2 A_v^2 + S_{a,\rm LNA}} \tag{A.2}$$

$$F_{\rm LNA} = \frac{(S_i/N_i)_{\rm LNA}}{(S_o/N_o)_{\rm LNA}} = 1 + \frac{S_{a,\rm LNA}}{\overline{V_{R_s}^2}A_v^2\left(\dfrac{R_{\rm in}}{R_s+R_{\rm in}}\right)^2}. \tag{A3}$$

$$\left(\frac{S_i}{N_i}\right)_{\text{new}} = \frac{V_{\text{in}}^2\left(\frac{R_p||R_{\text{in}}}{R_s+R_p||R_{\text{in}}}\right)^2}{\overline{V_{R_s}^2}\left(\frac{R_p||R_{\text{in}}}{R_s+R_p||R_{\text{in}}}\right)^2} \tag{A.4}$$

$$\left(\frac{S_o}{N_o}\right)_{\text{new}} = \frac{V_{\text{in}}^2\left(\frac{R_p||R_{\text{in}}}{R_s+R_p||R_{\text{in}}}\right)^2 A_v^2}{\overline{V_{R_s}^2}\left(\frac{R_p||R_{\text{in}}}{R_s+R_p||R_{\text{in}}}\right)^2 A_v^2+\overline{V_{R_p}^2}\left(\frac{R_s||R_{\text{in}}}{R_p+R_s||R_{\text{in}}}\right)^2 A_v^2+S_{a,\text{LNA}}} \tag{A.5}$$

$$F_{\text{new}} = \frac{(S_i/N_i)_{\text{new}}}{(S_o/N_o)_{\text{new}}} = \frac{\overline{V_{R_s}^2}\left(\frac{R_p||R_{\text{in}}}{R_s+R_p||R_{\text{in}}}\right)^2+\overline{V_{R_p}^2}\left(\frac{R_s||R_{\text{in}}}{R_p+R_s||R_{\text{in}}}\right)^2+\frac{S_{a,\text{LNA}}}{A_v^2}}{\overline{V_{R_s}^2}\left(\frac{R_p||R_{\text{in}}}{R_s+R_p||R_{\text{in}}}\right)^2} = 1+\frac{R_s}{R_p}+\frac{\frac{S_{a,\text{LNA}}}{A_v^2}}{\overline{V_{R_s}^2}\left(\frac{R_s||R_p||R_{\text{in}}}{R_s}\right)^2} \tag{A.6}$$

R_s is source resistance and also equivalent to R_{ant} in (16). The LNA is composed of a noiseless LNA and added noise $S_{a,\text{LNA}}$. The LNA has voltage gain A_v and its input resistance is R_{in}. The noise model of the PA's output is a parallel resistance R_p at the LNA input. A new noise factor with a PA (F_{new}) can found as shown in (A.4)–(A.6) at the top of this page, where

$$\frac{R_s||R_{\text{in}}}{R_p+R_s||R_{\text{in}}} = \frac{R_s||R_p||R_{\text{in}}}{R_p} \tag{A.7}$$

$$\frac{R_p||R_{\text{in}}}{R_s+R_p||R_{\text{in}}} = \frac{R_s||R_p||R_{\text{in}}}{R_s}. \tag{A.8}$$

Using (A.3) and under assumption that $R_s = R_{\text{in}}$,

$$\begin{aligned} F_{\text{new}} &= 1+\frac{R_s}{R_p}+\frac{\left(\frac{R_s}{R_s+R_{\text{in}}}\right)^2(F_{\text{LNA}}-1)}{\left(\frac{R_s||R_p||R_{\text{in}}}{R_s}\right)^2} \\ &= 1+\frac{R_s}{R_p}+\frac{(F_{\text{LNA}}-1)}{\left(\frac{R_p}{\frac{R_s}{2}+R_p}\right)^2}. \end{aligned} \tag{A.9}$$

Fig. 7 depicts the NF degradation due to the PA. For a fixed R_p, the NF_{new} is nearly a sum of NF_{LNA} and a constant in the plot. When R_p is comparable to R_s, the NF_{new} is much worse than NF_{LNA}, but as R_p becomes much bigger than R_s, the degradation becomes unnoticeable. The microtransceiver' LNA has 3.4-dB NF [27] and the PA's output resistance is 360 Ω. Hence, from (A.9), NF_{new} is expected to be 4.0 dB. If $R_s/2R_p \ll 1$, which is true with the high Q output transformer, F_{new} can be further simplified to

$$F_{\text{new}} \approx 1+\frac{R_s}{R_p}+(F-1)\left(1+\frac{R_s}{R_p}\right) = F\left(1+\frac{R_s}{R_p}\right). \tag{A.10}$$

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